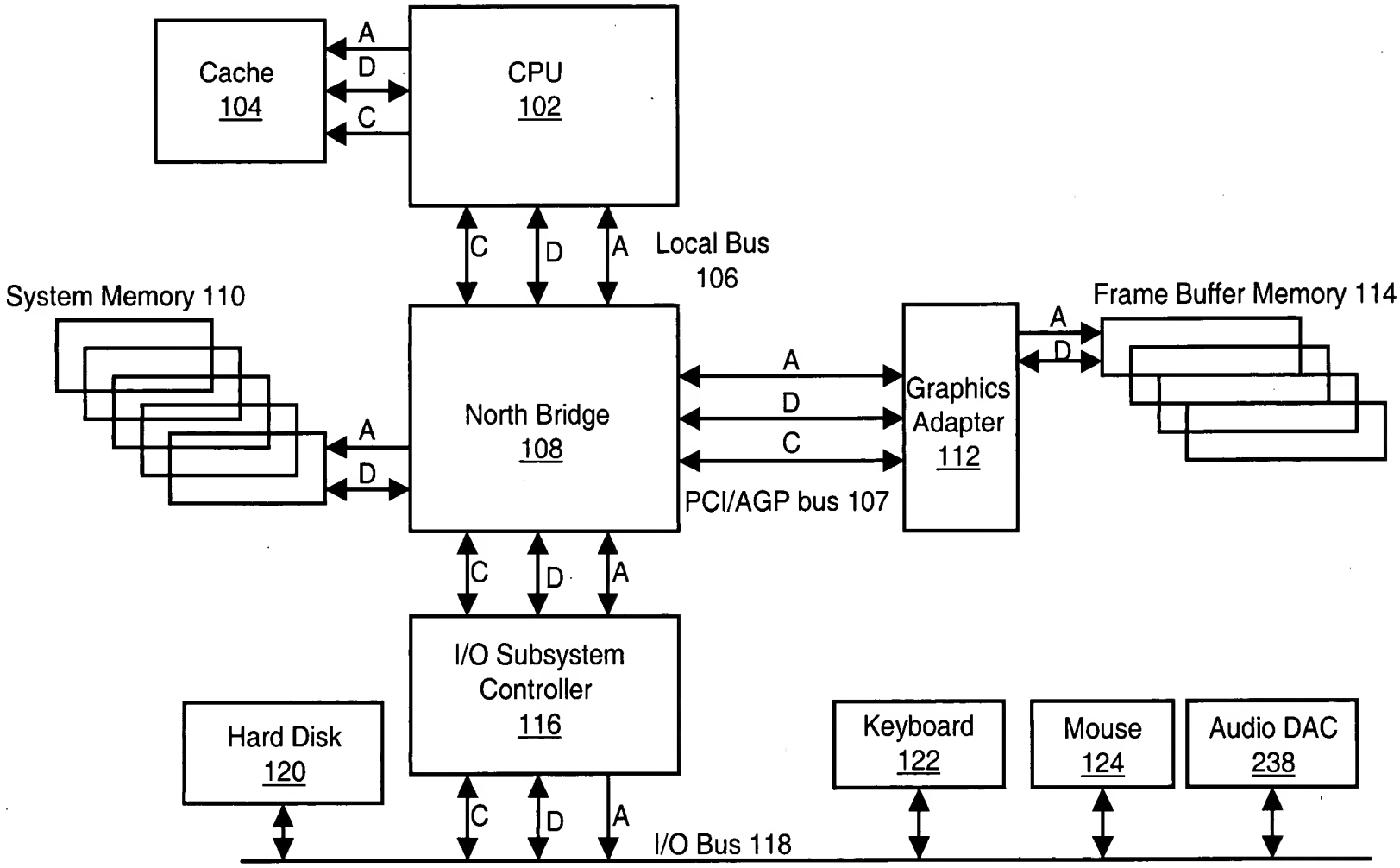


Fig 1
Prior Art

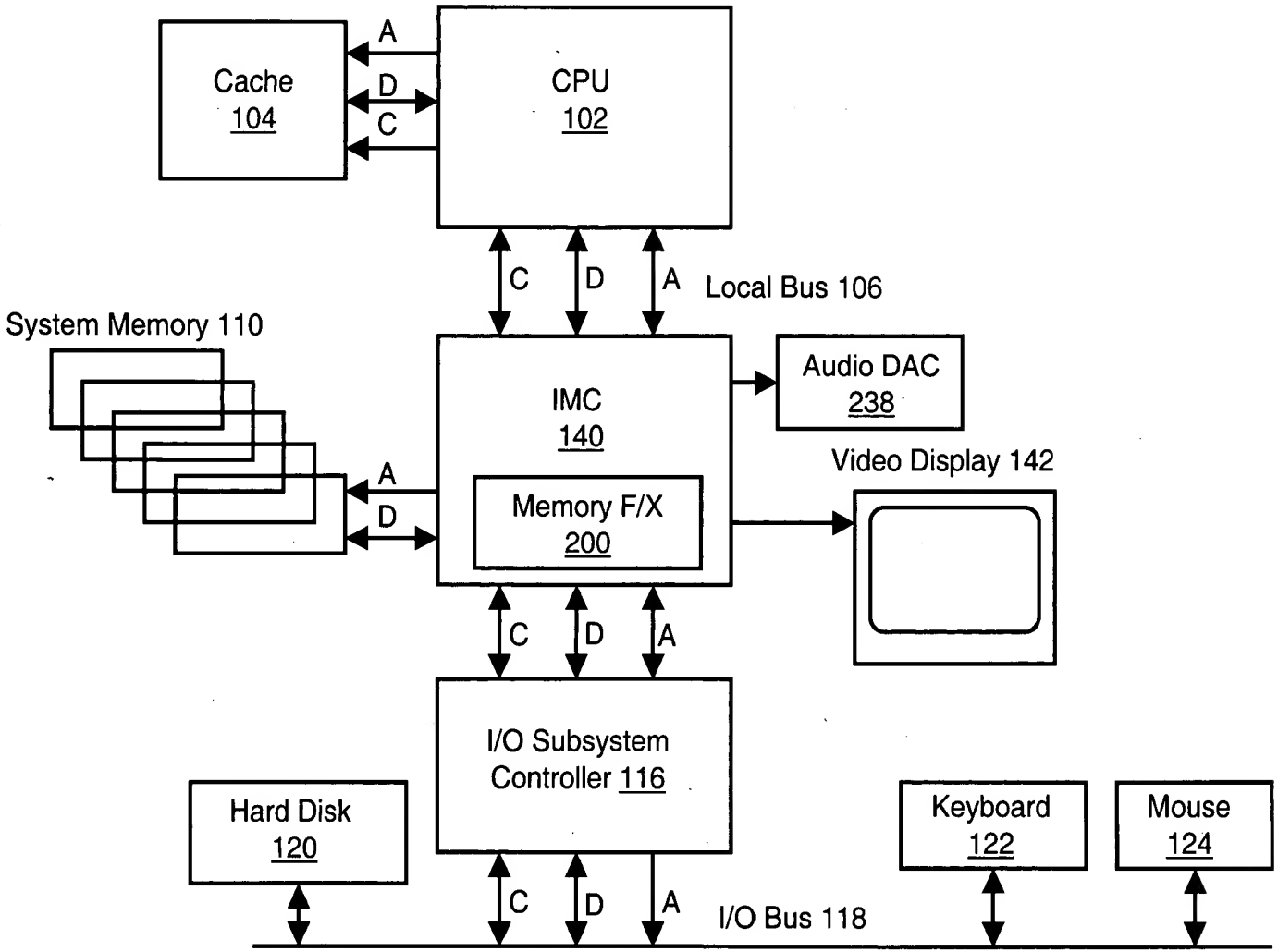


Fig. 2A

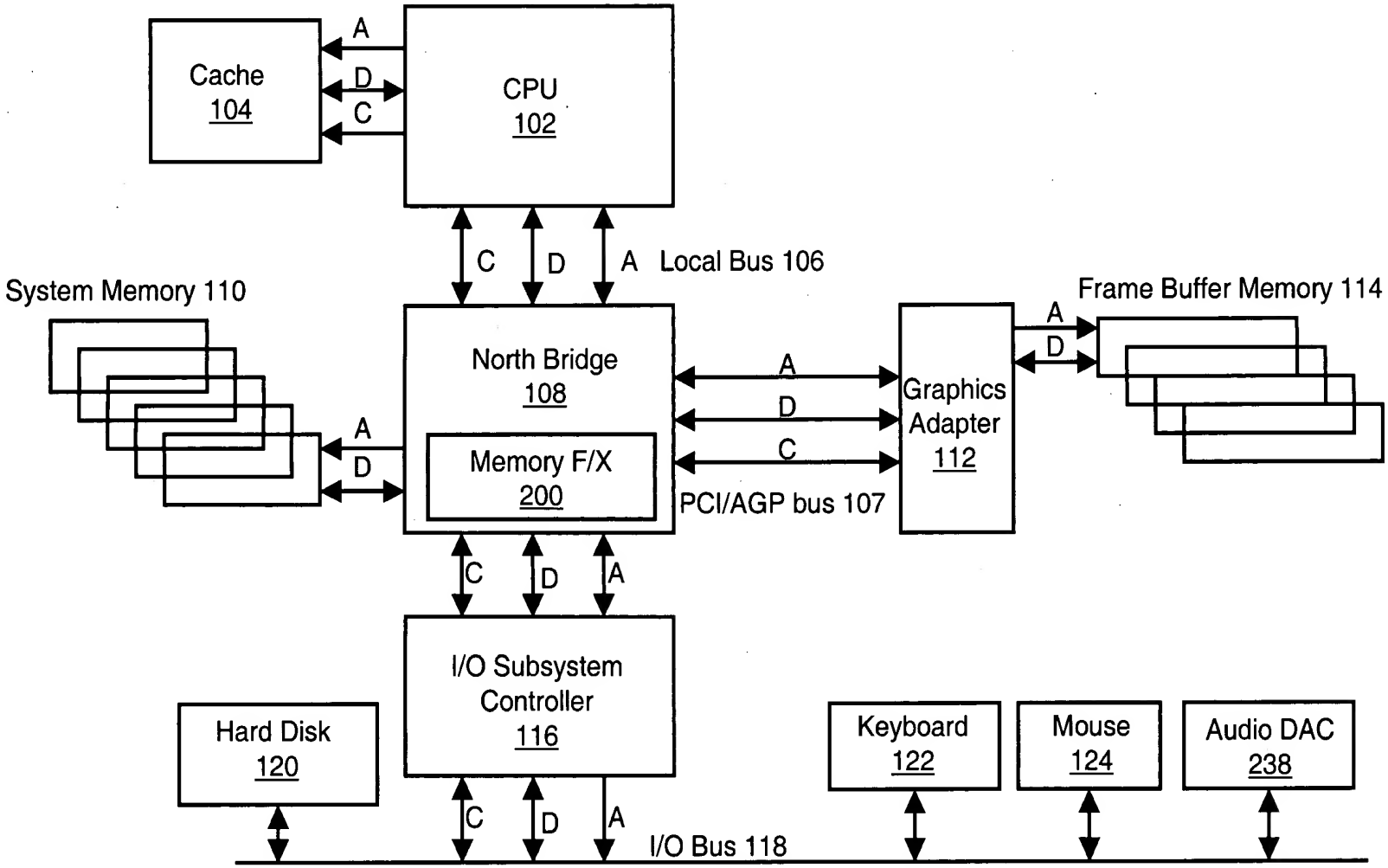

Cache
104
A
D
C
CPU
102
C
D
A
Local Bus 106
System Memory 110
North Bridge
108
Memory F/X
200
A
D
A
D
C
PCI/AGP bus 107
Graphics
Adapter
112
A
D
Frame Buffer Memory 114
C
D
A
I/O Subsystem
Controller
116
Hard Disk
120
Keyboard
122
Mouse
124
Audio DAC
238
C
D
A
I/O Bus 118

Fig. 2B

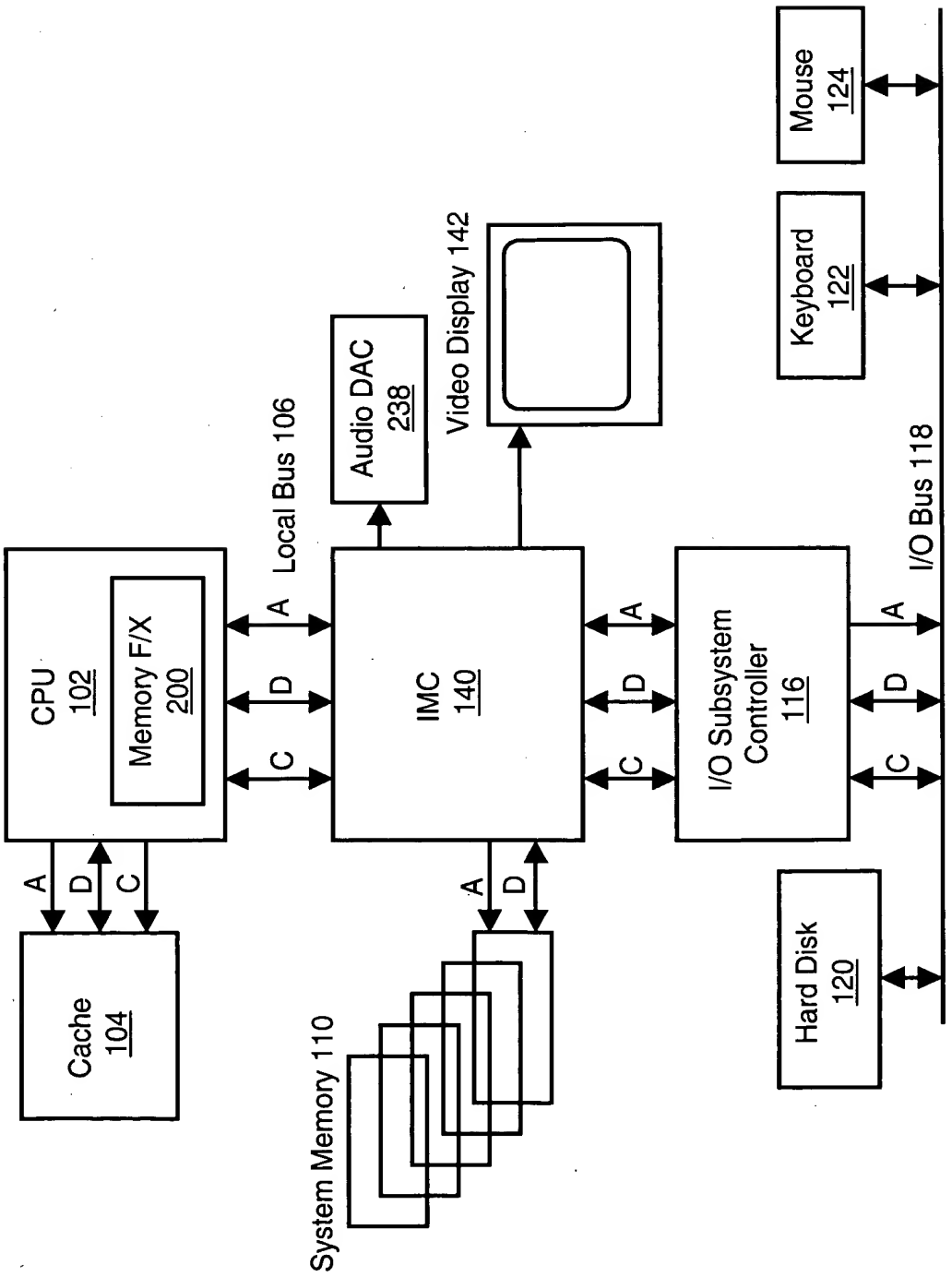

CPU
102
Memory F/X
200
Cache
104
A
D
C
Local Bus 106
IMC
140
Audio DAC
238
Video Display 142
System Memory 110
I/O Subsystem
Controller
116
I/O Bus 118
Mouse
124
Keyboard
122
Hard Disk
120

Fig. 2C

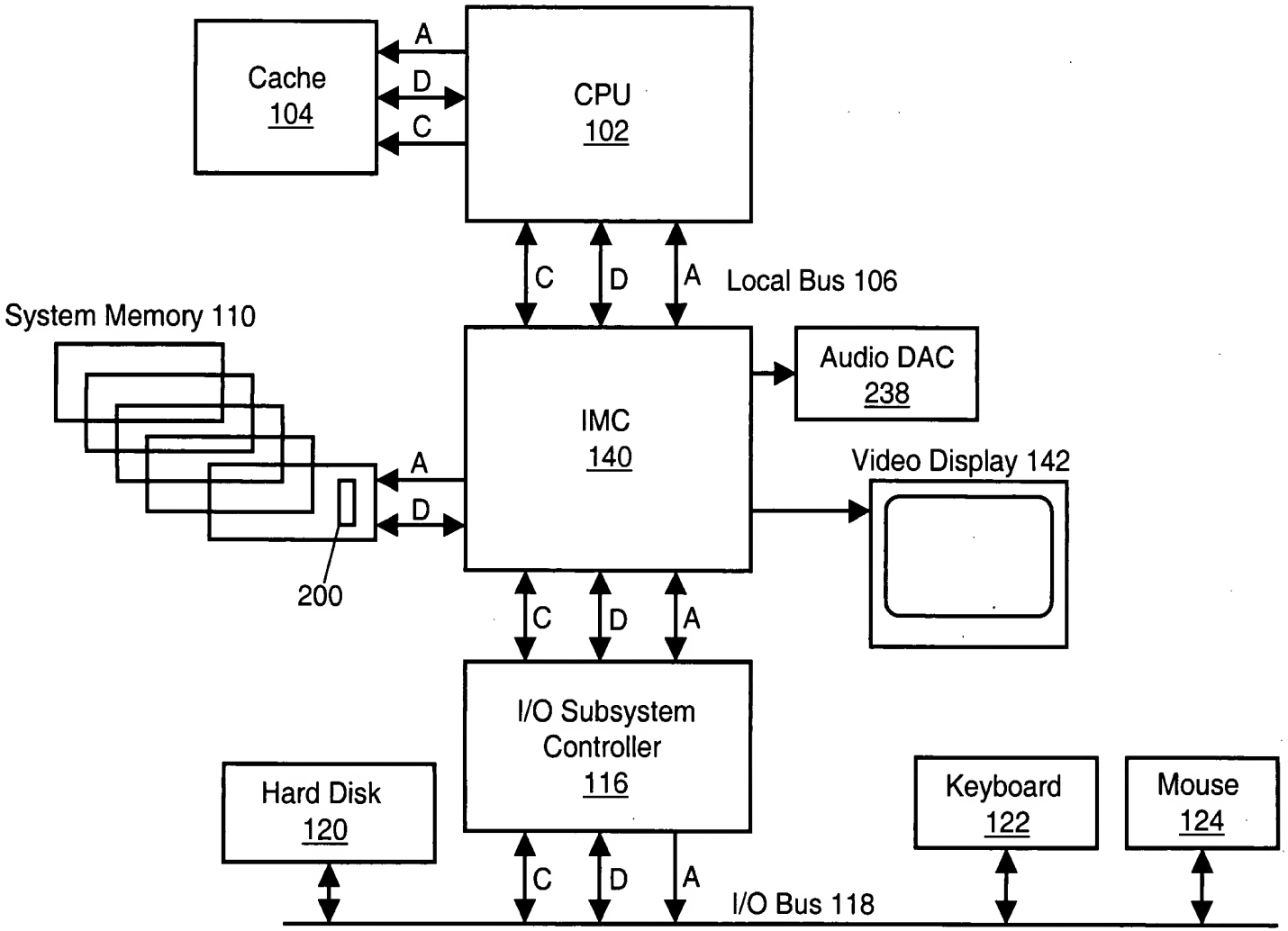

Cache
104
A
D
C
CPU
102
C
D
A
Local Bus 106
System Memory 110
IMC
140
Audio DAC
238
Video Display 142
A
D
200
C
D
A
I/O Subsystem
Controller
116
Hard Disk
120
Keyboard
122
Mouse
124
C
D
A
I/O Bus 118

Fig. 2D

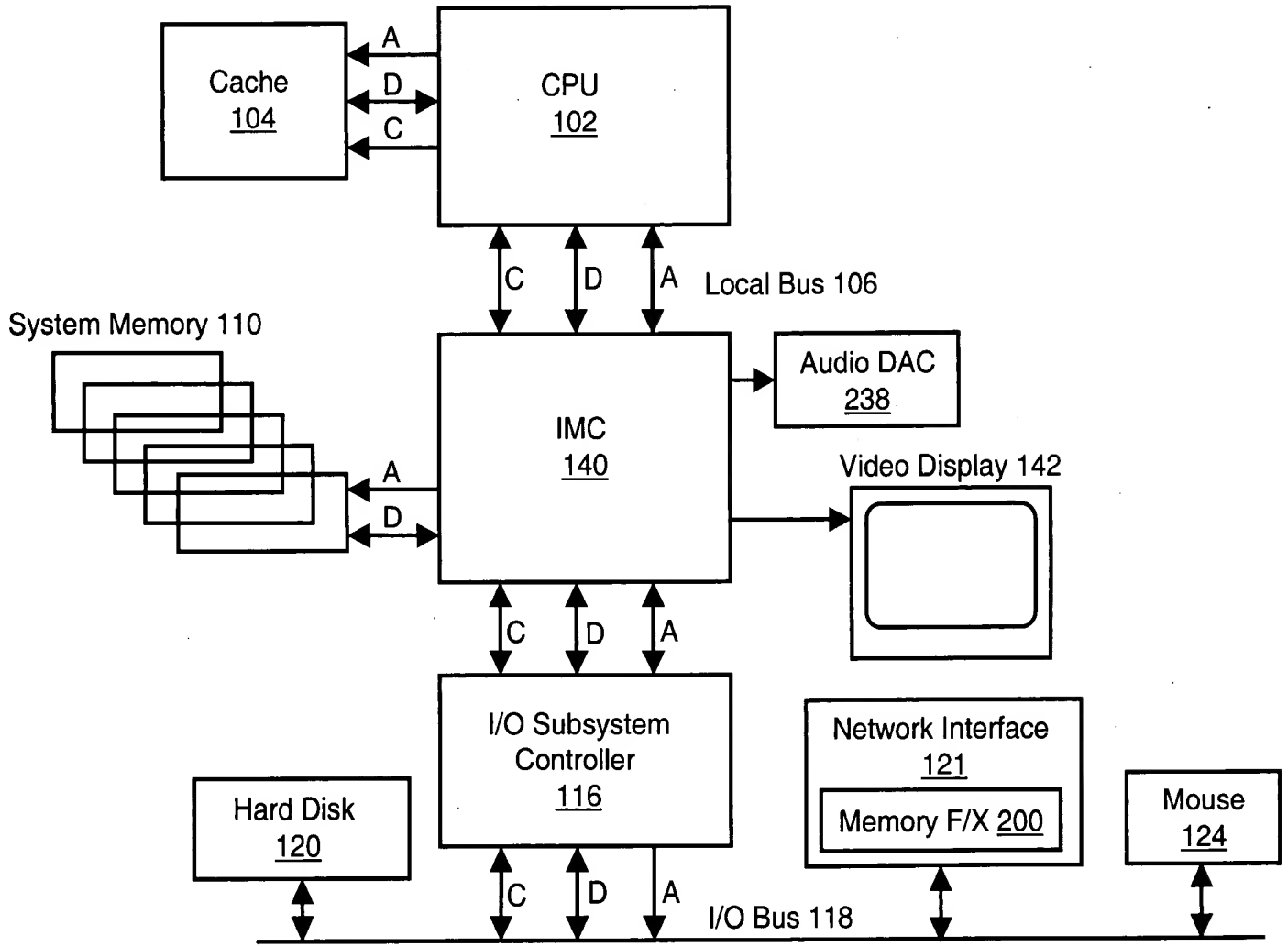

Cache
104
A
D
C
CPU
102
C
D
A
Local Bus 106
System Memory 110
Audio DAC
238
IMC
140
A
D
Video Display 142
C
D
A
I/O Subsystem
Controller
116
Network Interface
121
Memory F/X 200
Hard Disk
120
Mouse
124
C
D
A
I/O Bus 118

Fig. 2E

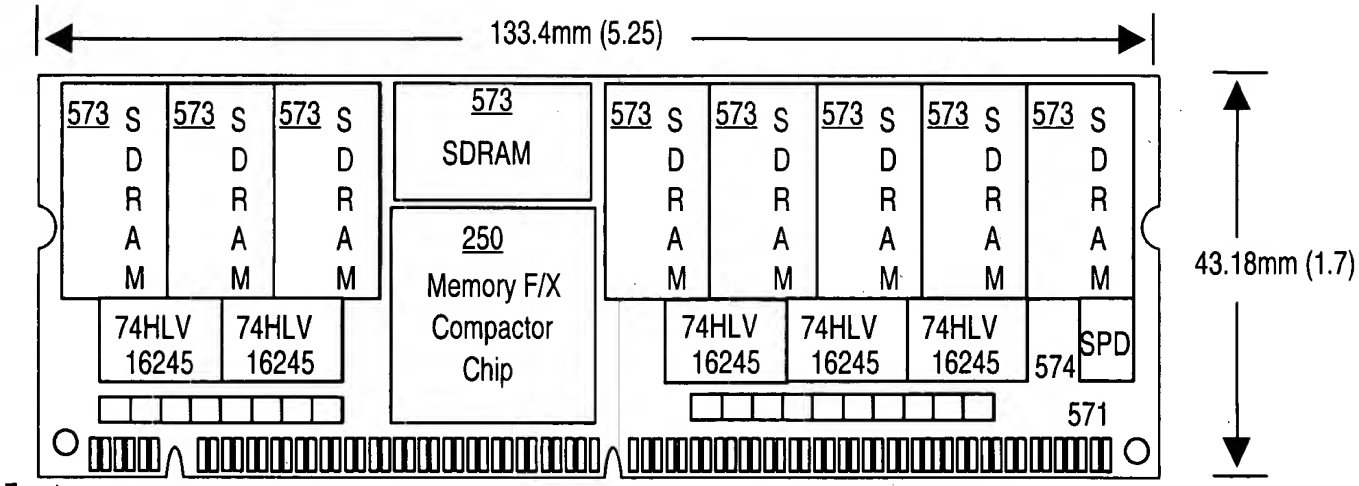

133.4mm (5.25)
573 SDRAM
250 Memory F/X Compactor Chip
74HLV 16245
74HLV 16245
74HLV 16245
74HLV 16245
74HLV 16245
SPD
574
571
43.18mm (1.7)
Front

Fig. 3a

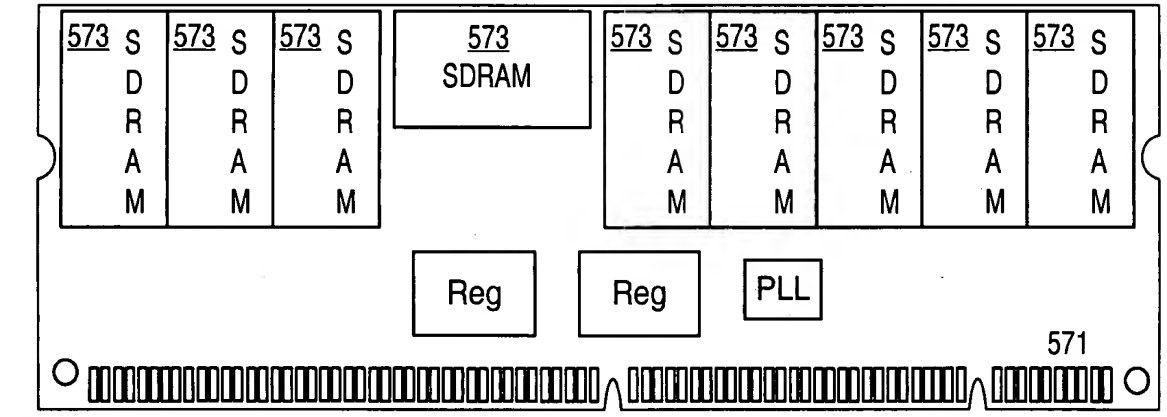
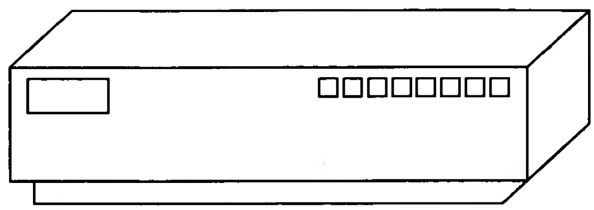

573 SDRAM
Reg
Reg
PLL
571
Back

Fig. 3b



Router 130

Fig. 4

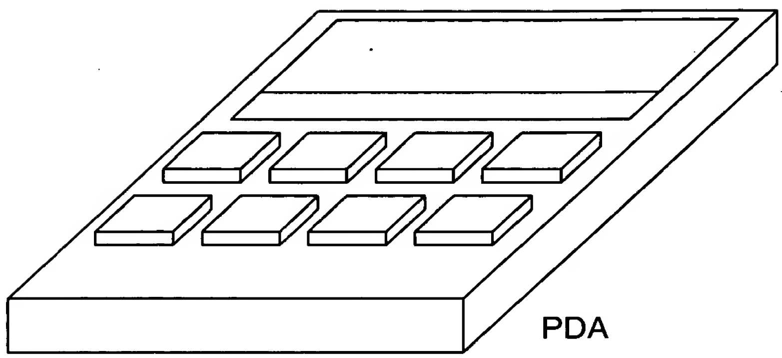


Fig. 5

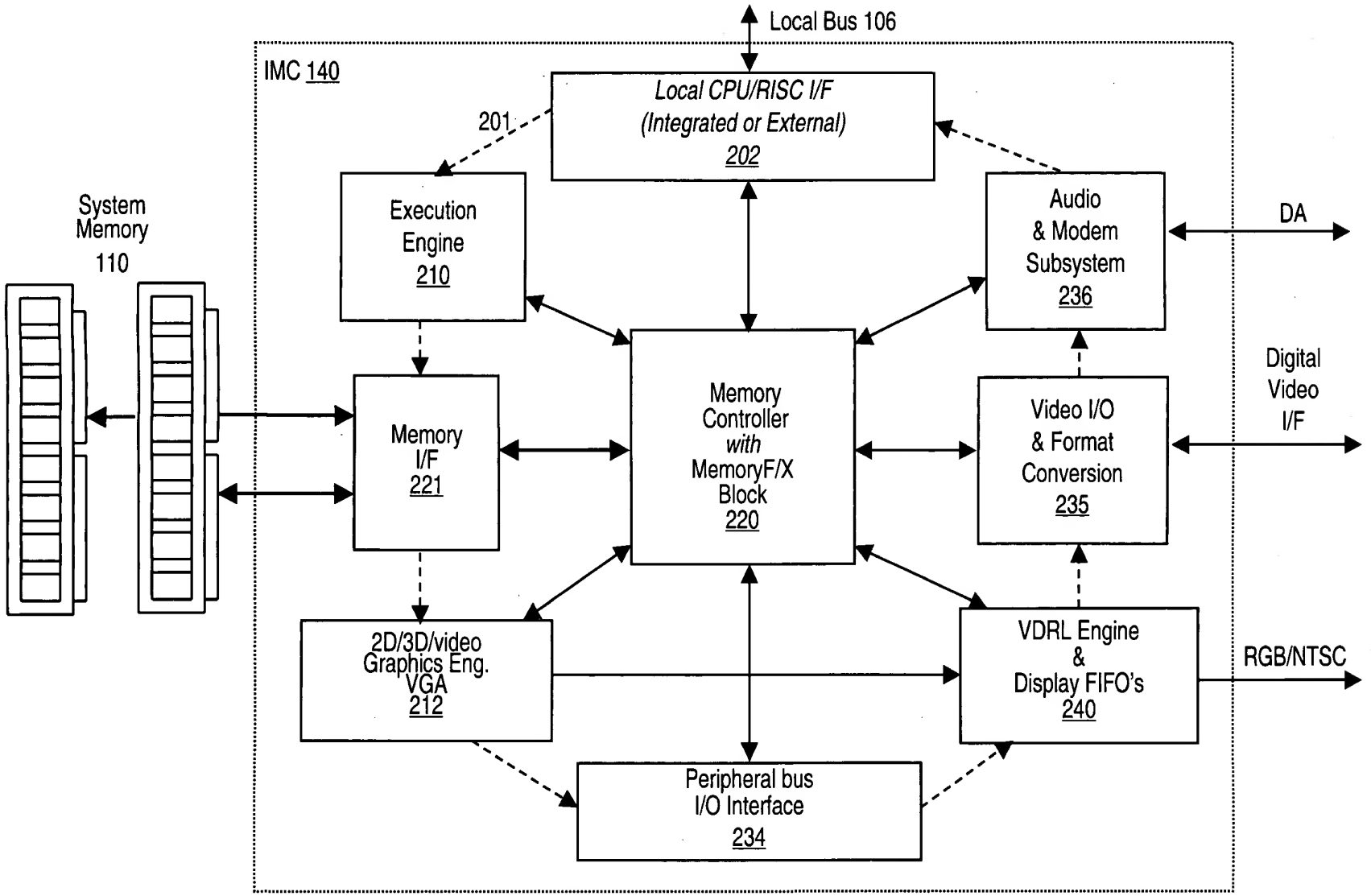

Local Bus 106
IMC 140
Local CPU/RISC I/F
(Integrated or External)
202
201
System
Memory
110
Execution
Engine
210
Audio
& Modem
Subsystem
236
DA
Memory
I/F
221
Memory
Controller
with
MemoryF/X
Block
220
Video I/O
& Format
Conversion
235
Digital
Video
I/F
2D/3D/video
Graphics Eng.
VGA
212
VDRL Engine
&
Display FIFO's
240
RGB/NTSC
Peripheral bus
I/O Interface
234

Fig. 6

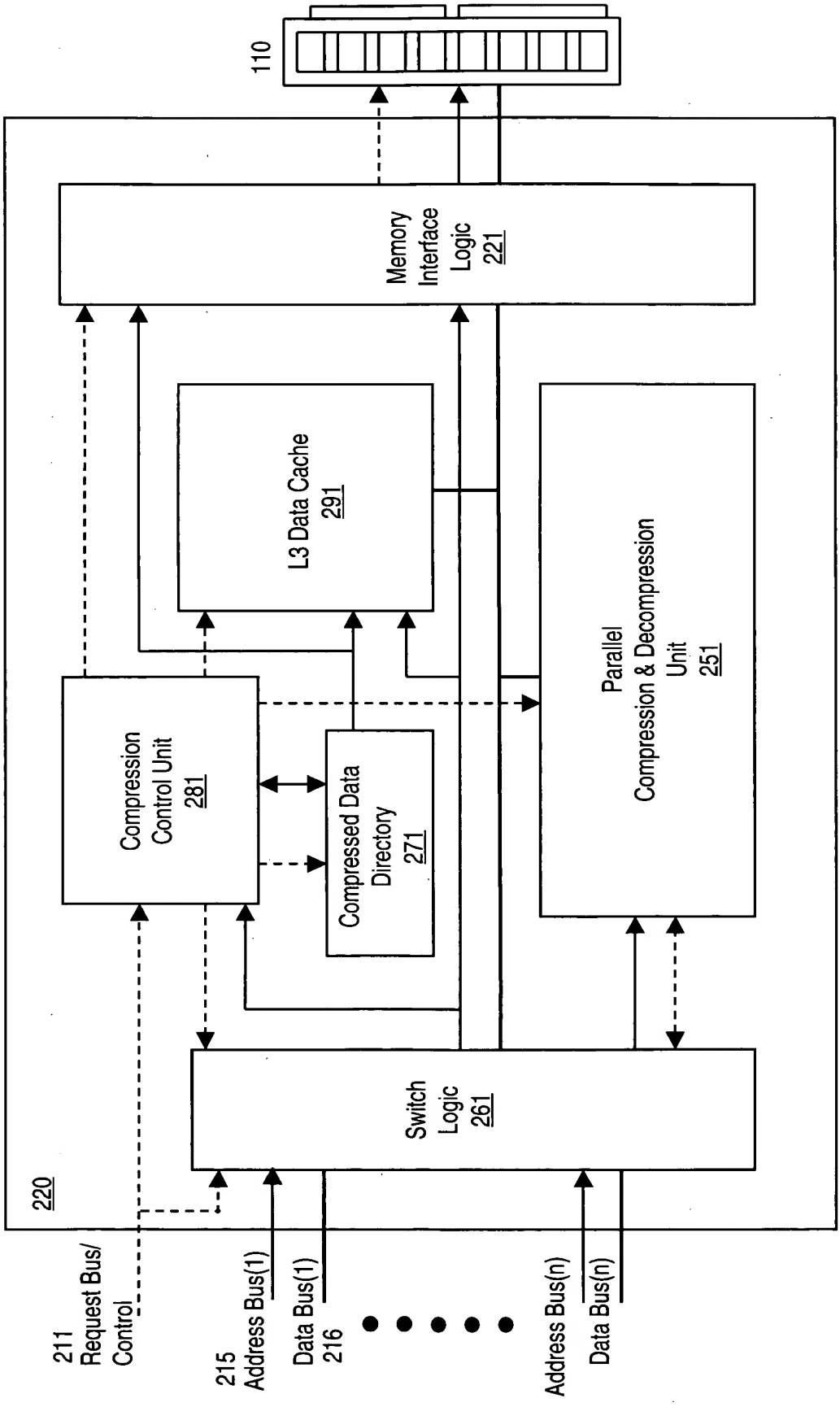

110
Memory Interface Logic 221
L3 Data Cache 291
Compression Control Unit 281
Compressed Data Directory 271
Parallel Compression & Decompression Unit 251
Switch Logic 261
220
211 Request Bus/ Control
215 Address Bus(1)
Data Bus(1) 216
Address Bus(n)
Data Bus(n)

Fig. 7

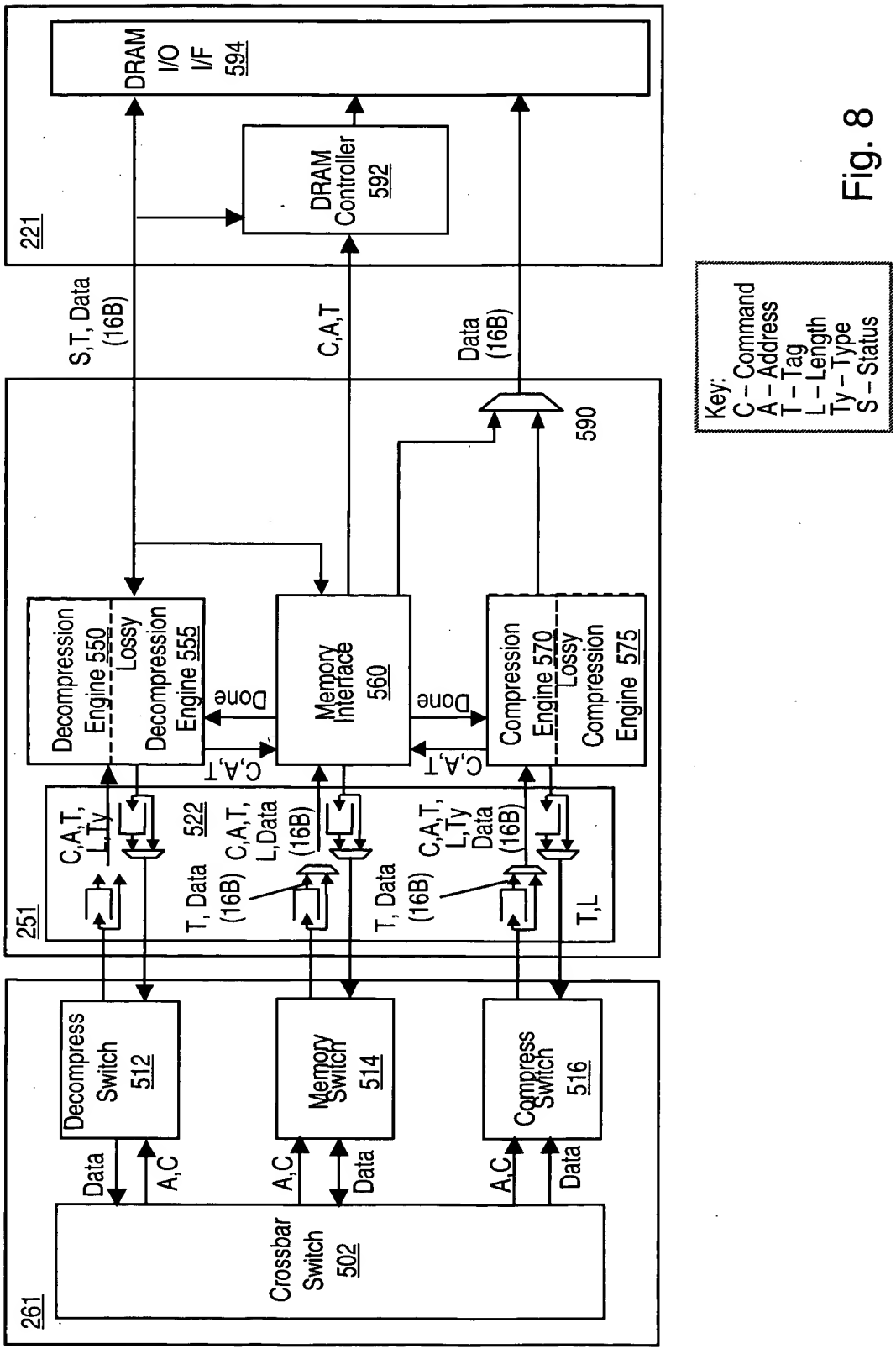

DRAM I/O I/F 594
DRAM Controller 592
221
S,T, Data (16B)
C,A,T
Data (16B)
590
Key:
C – Command
A – Address
T – Tag
L – Length
Ty – Type
S – Status
Decompression Engine 550
Lossy Decompression Engine 555
Memory Interface 560
Compression Engine 570
Lossy Compression Engine 575
Done
C,A,T
C,A,T, L,Ty
522
C,A,T, L,Data (16B)
C,A,T, L,Ty Data (16B)
T, Data (16B)
T,L
251
Decompress Switch 512
Memory Switch 514
Compress Switch 516
Data
A,C
Crossbar Switch 502
261

Fig. 8

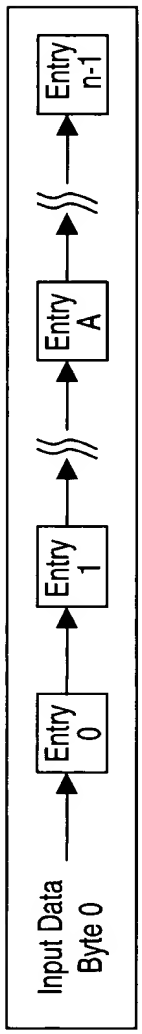


Fig. 9a
(Prior Art)

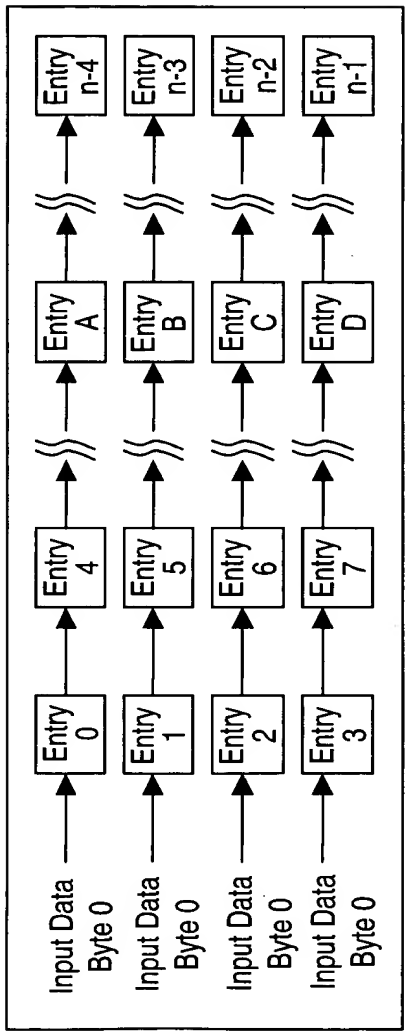


Fig. 9b
(New Art)

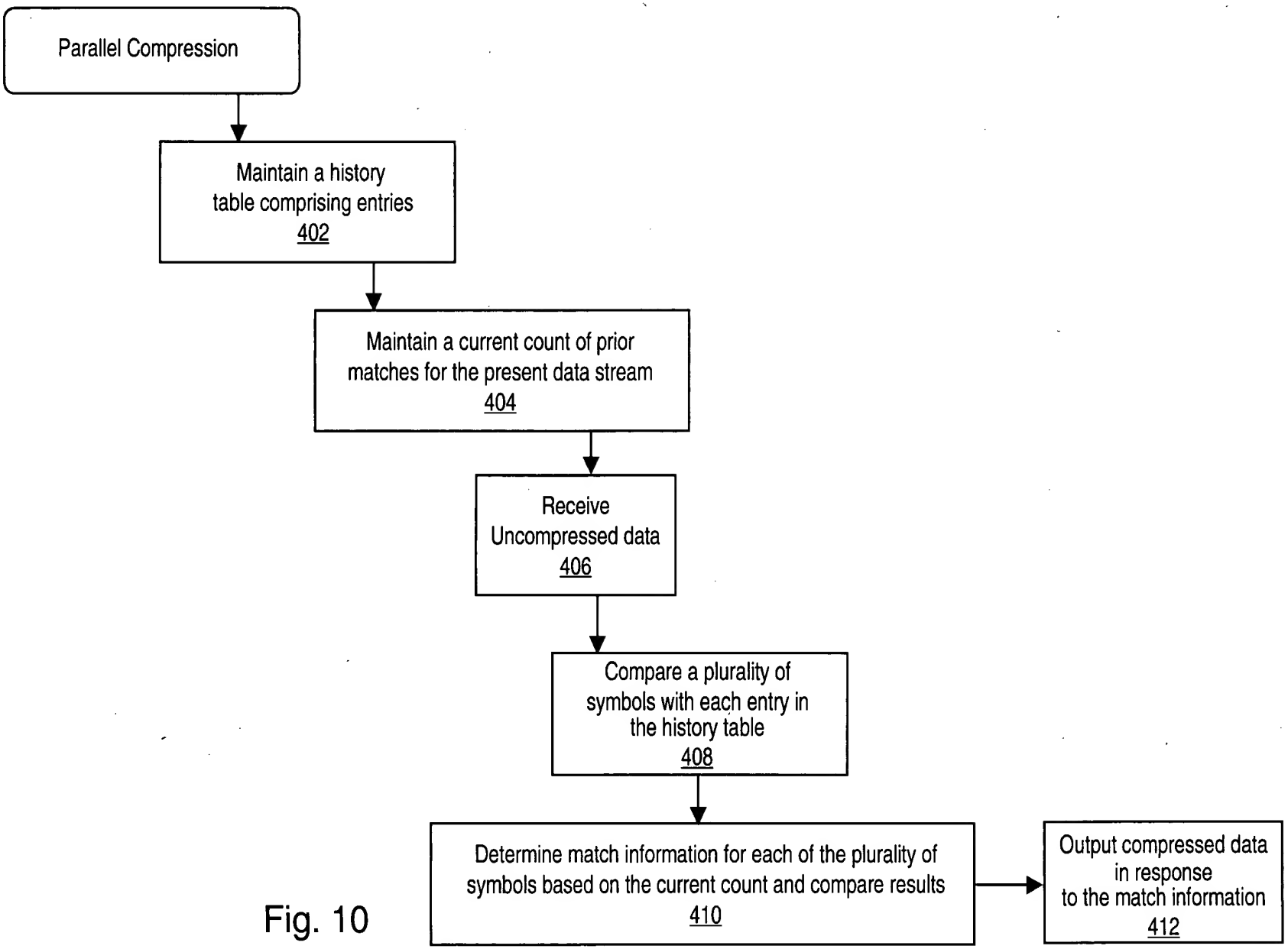

Parallel Compression
Maintain a history table comprising entries 402
Maintain a current count of prior matches for the present data stream 404
Receive Uncompressed data 406
Compare a plurality of symbols with each entry in the history table 408
Determine match information for each of the plurality of symbols based on the current count and compare results 410
Output compressed data in response to the match information 412

Fig. 10

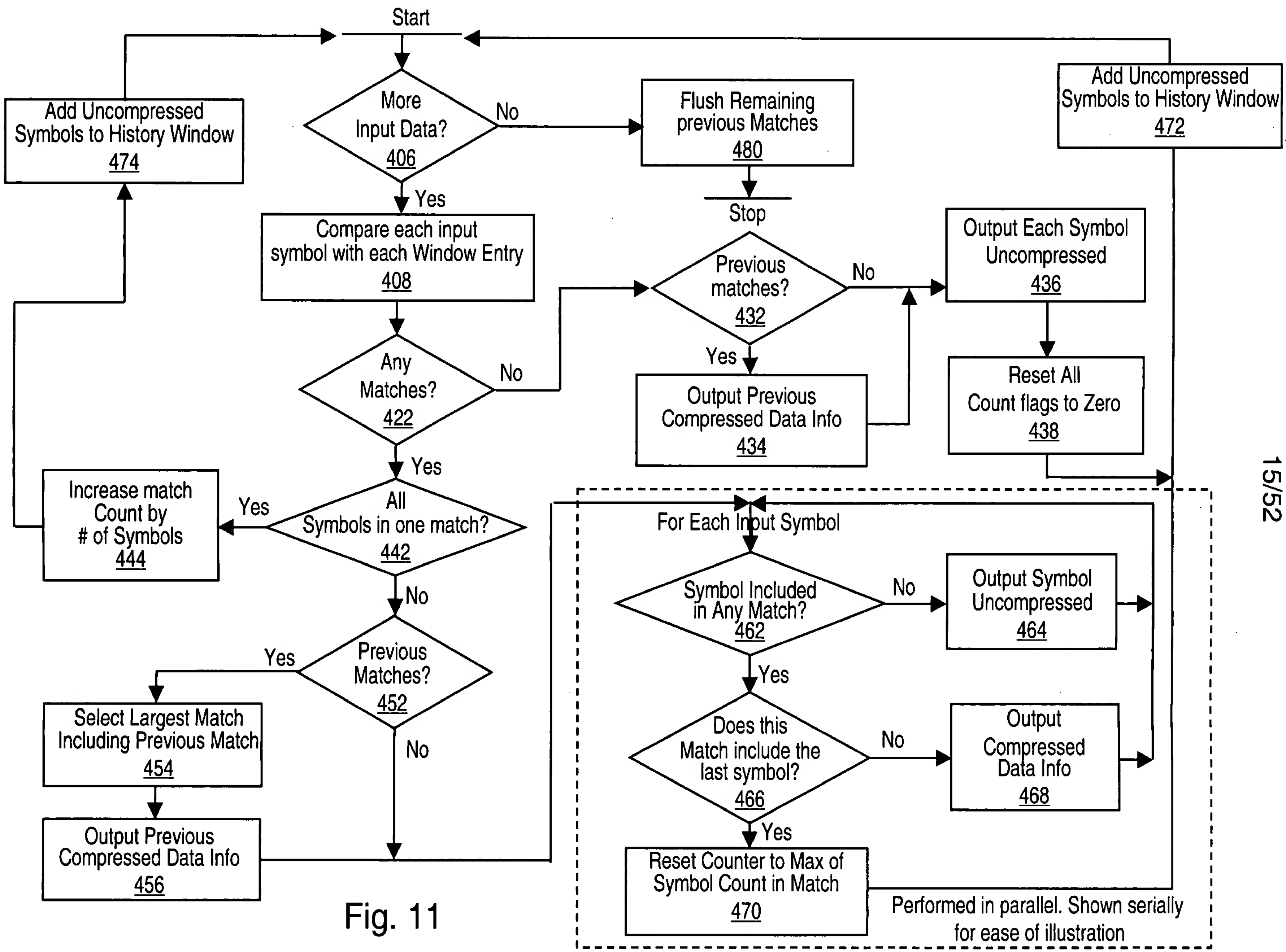


Fig. 11

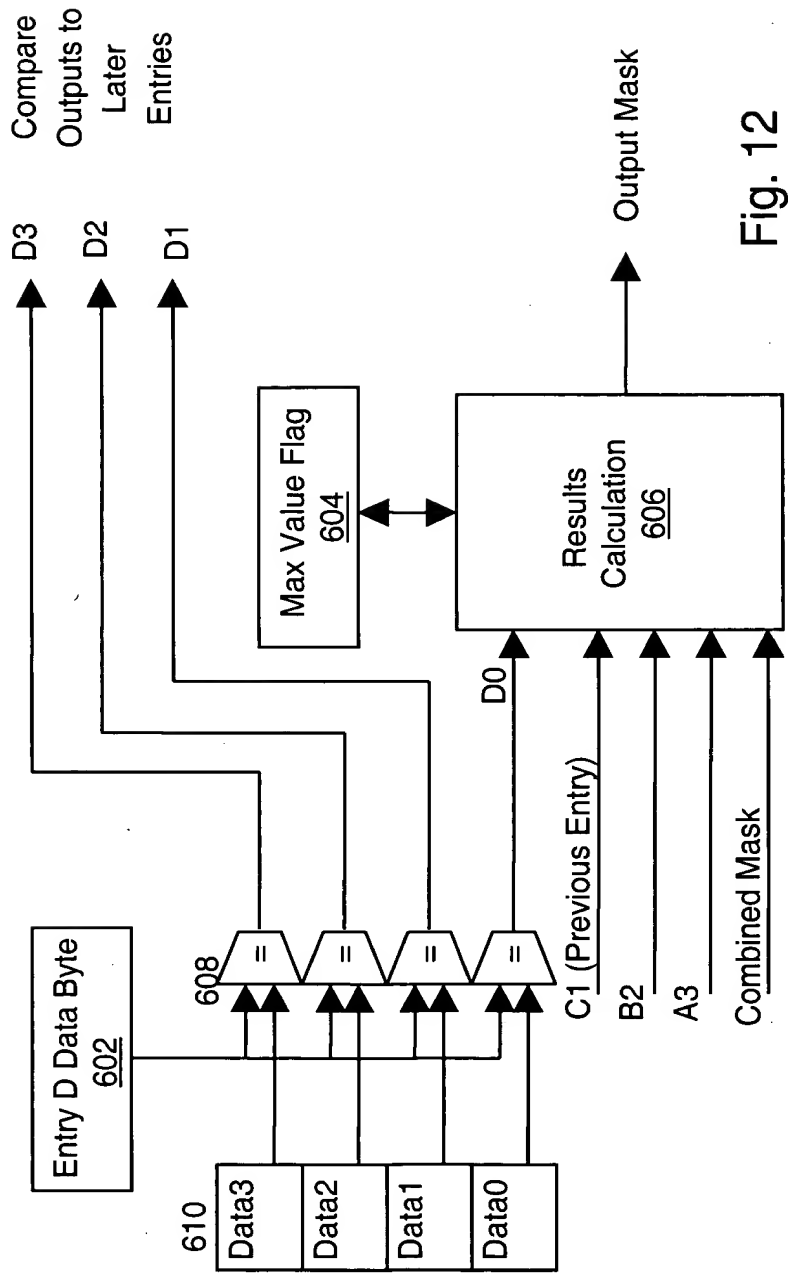

Compare Outputs to Later Entries
D3
D2
D1
Output Mask
Max Value Flag 604
Results Calculation 606
Entry D Data Byte 602
608
=
=
=
=
D0
C1 (Previous Entry)
B2
A3
Combined Mask
610
Data3
Data2
Data1
Data0

Fig. 12

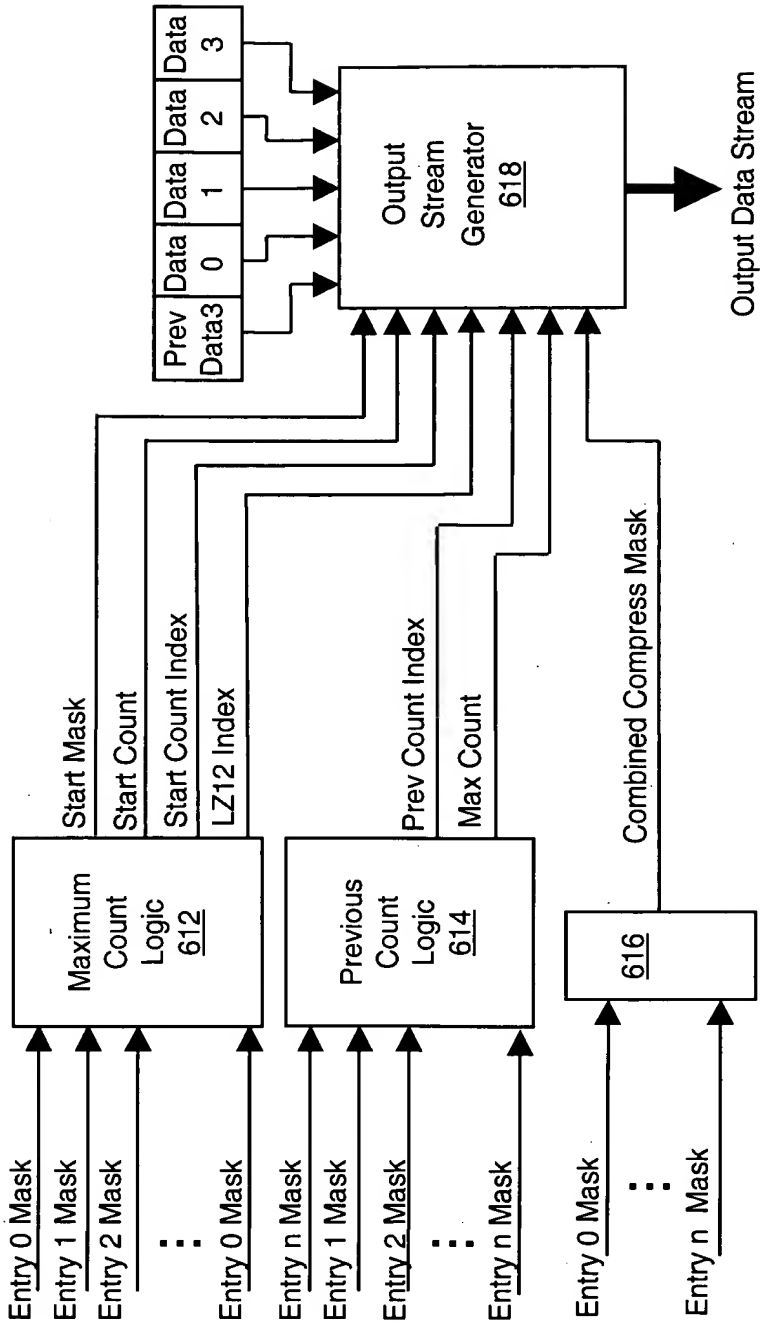

Entry 0 Mask
Entry 1 Mask
Entry 2 Mask
Entry 0 Mask
Maximum Count Logic 612
Start Mask
Start Count
Start Count Index
LZ12 Index
Entry n Mask
Entry 1 Mask
Entry 2 Mask
Entry n Mask
Previous Count Logic 614
Prev Count Index
Max Count
Entry 0 Mask
Entry n Mask
616
Combined Compress Mask
Prev Data3
Data 0
Data 1
Data 2
Data 3
Output Stream Generator 618
Output Data Stream

Fig. 13

Input Matches				Output
D0	C1	B2	A3	Mask
1	1	1	1	1111
1	1	1	0	1110
1	1	0	1	1101
1	1	0	0	1100
1	0	1	1	1011
1	0	1	0	1010
1	0	0	1	1001
1	0	0	0	1000
0	1	1	1	0111
0	1	1	0	0110
0	1	0	1	0101
0	1	0	0	0100
0	0	1	1	0011
0	0	1	0	0010
0	0	0	1	0001
0	0	0	0	0000

Figure 14a

Combined Mask	Count
0000	0
0001	1
0010	0
0011	2
0100	0
0101	1
0110	0
0111	3
1000	0
1001	1
1010	0
1011	2
1100	0
1101	1
1110	0
1111	Count+4

Figure 14b

Output Masks	Combined Mask
M1234 | 4321 &~M1	0001
432 & ~M12	0010
43 & ~M123	0100
4 & ~M1234	1000
First valid row determines Combined Mask Output	
M-Max Count Flag 1-1st Symbol Match 2-2nd Symbol Match 3-3rd Symbol Match 4-4th Symbol Match	

Fig. 14c

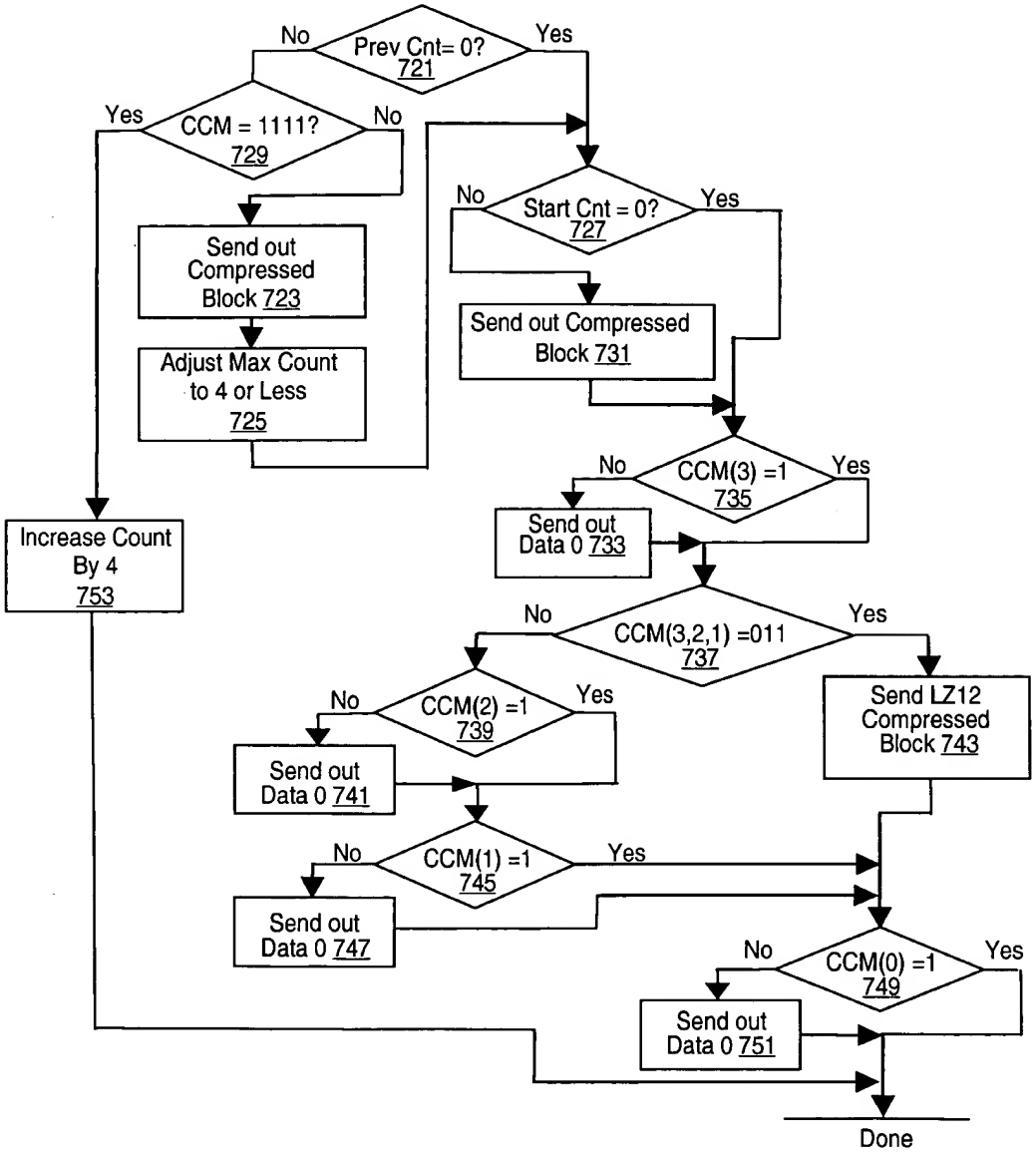

Prev Cnt= 0? 721
No
Yes
CCM = 1111? 729
Yes
No
Send out Compressed Block 723
Adjust Max Count to 4 or Less 725
Increase Count By 4 753
Start Cnt = 0? 727
No
Yes
Send out Compressed Block 731
CCM(3) =1 735
No
Yes
Send out Data 0 733
CCM(3,2,1) =011 737
No
Yes
Send LZ12 Compressed Block 743
CCM(2) =1 739
No
Yes
Send out Data 0 741
CCM(1) =1 745
No
Yes
Send out Data 0 747
CCM(0) =1 749
No
Yes
Send out Data 0 751
Done

Fig. 15

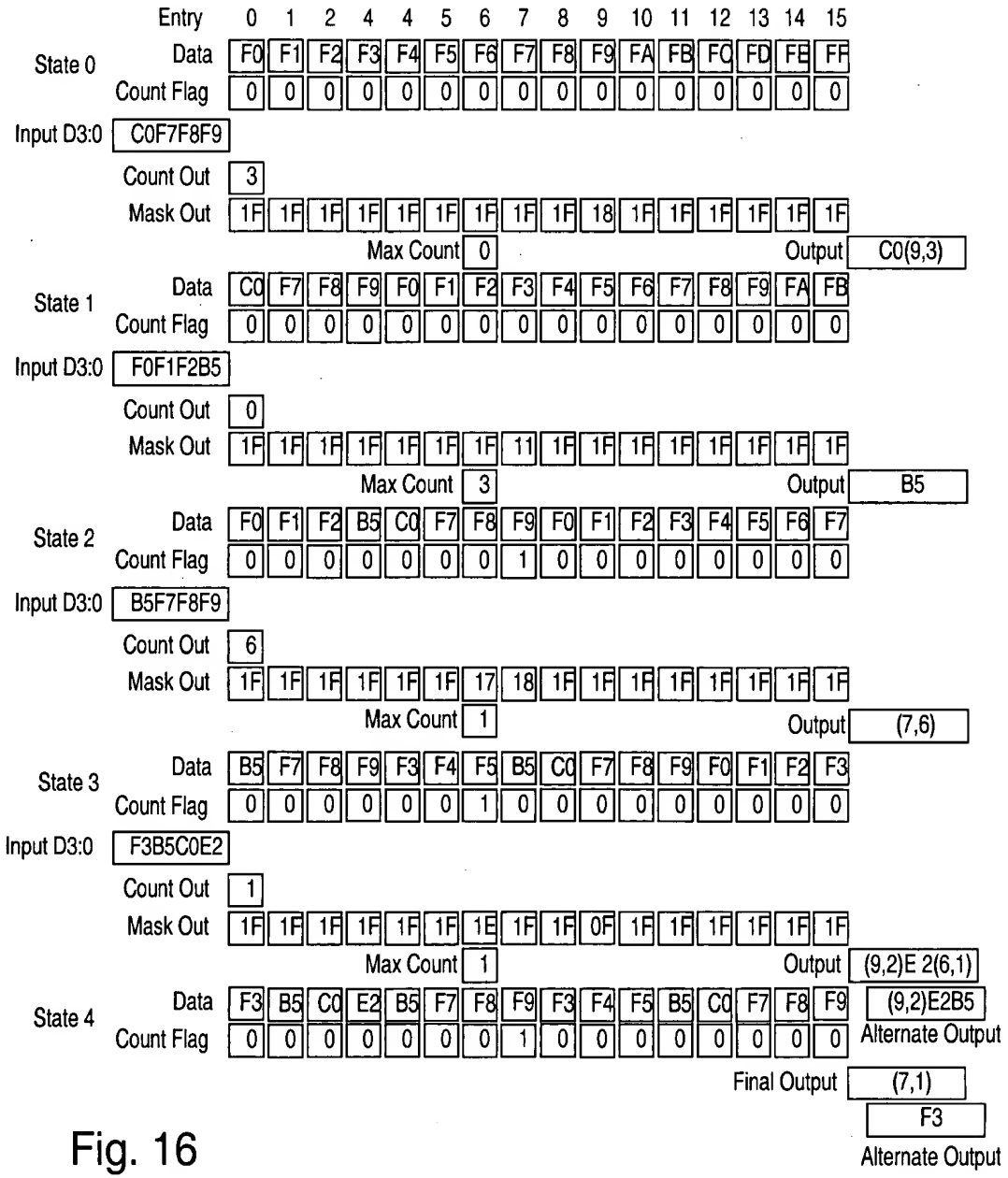

Entry 0 1 2 4 4 5 6 7 8 9 10 11 12 13 14 15
State 0
Data F0 F1 F2 F3 F4 F5 F6 F7 F8 F9 FA FB FC FD FE FF
Count Flag 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Input D3:0 C0F7F8F9
Count Out 3
Mask Out 1F 1F 1F 1F 1F 1F 1F 1F 1F 18 1F 1F 1F 1F 1F 1F
Max Count 0
Output C0(9,3)
State 1
Data C0 F7 F8 F9 F0 F1 F2 F3 F4 F5 F6 F7 F8 F9 FA FB
Count Flag 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Input D3:0 F0F1F2B5
Count Out 0
Mask Out 1F 1F 1F 1F 1F 1F 1F 11 1F 1F 1F 1F 1F 1F 1F 1F
Max Count 3
Output B5
State 2
Data F0 F1 F2 B5 C0 F7 F8 F9 F0 F1 F2 F3 F4 F5 F6 F7
Count Flag 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0
Input D3:0 B5F7F8F9
Count Out 6
Mask Out 1F 1F 1F 1F 1F 1F 17 18 1F 1F 1F 1F 1F 1F 1F 1F
Max Count 1
Output (7,6)
State 3
Data B5 F7 F8 F9 F3 F4 F5 B5 C0 F7 F8 F9 F0 F1 F2 F3
Count Flag 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0
Input D3:0 F3B5C0E2
Count Out 1
Mask Out 1F 1F 1F 1F 1F 1F 1E 1F 1F 0F 1F 1F 1F 1F 1F 1F
Max Count 1
Output (9,2)E 2(6,1)
State 4
Data F3 B5 C0 E2 B5 F7 F8 F9 F3 F4 F5 B5 C0 F7 F8 F9
(9,2)E2B5
Alternate Output
Count Flag 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0
Final Output (7,1)
F3
Alternate Output

Fig. 16

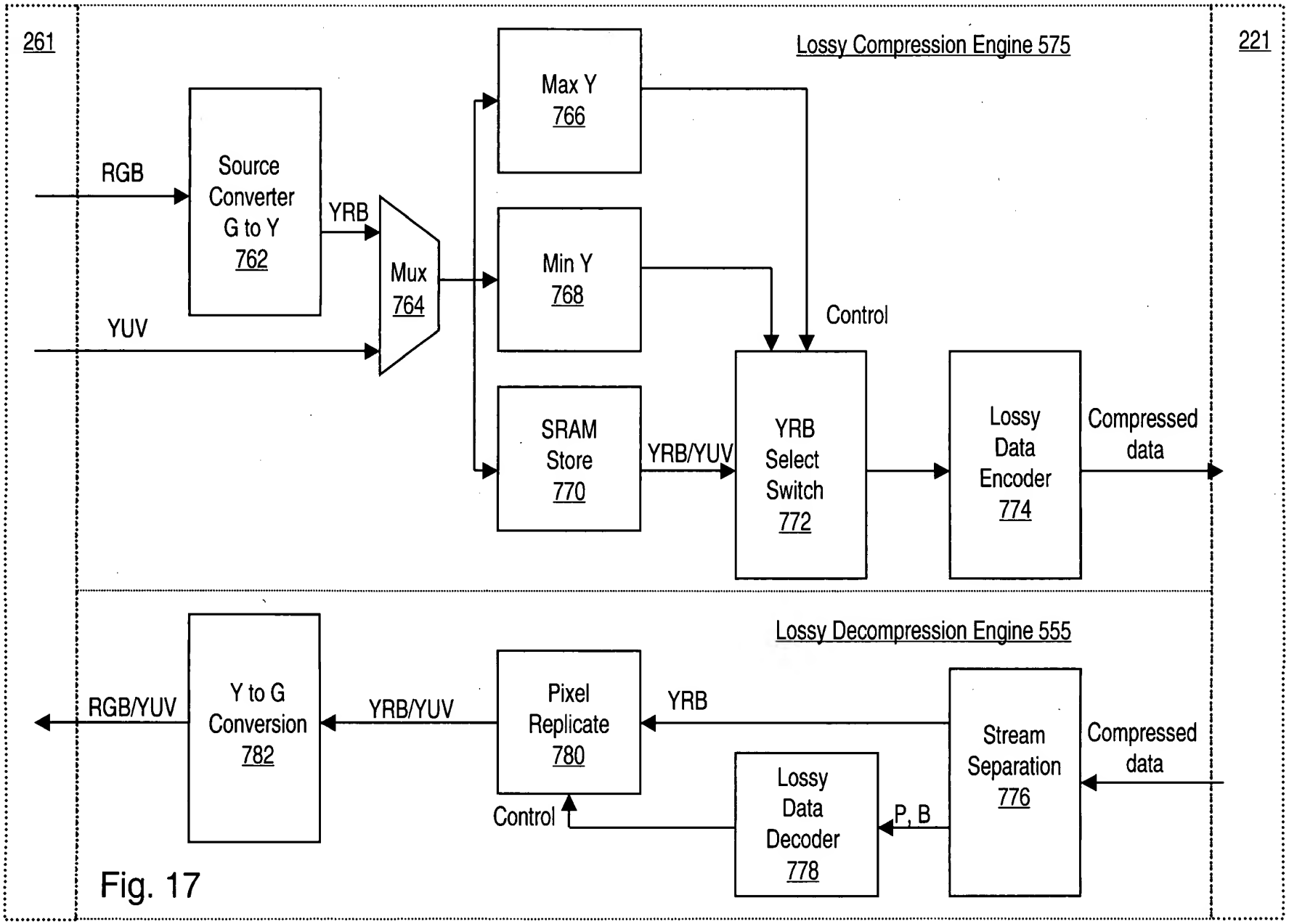

261
221
Lossy Compression Engine 575
RGB
Source Converter G to Y 762
YRB
Mux 764
YUV
Max Y 766
Min Y 768
SRAM Store 770
Control
YRB/YUV
YRB Select Switch 772
Lossy Data Encoder 774
Compressed data
Lossy Decompression Engine 555
RGB/YUV
Y to G Conversion 782
YRB/YUV
Pixel Replicate 780
YRB
Stream Separation 776
Compressed data
Control
Lossy Data Decoder 778
P, B

Fig. 17

Ymax = Ymin	1 color	Ymax	Ymax	Rmax	Bmax	11			3 Bytes
		6 bits	6 bits	5 bits	5 bits	2 bits			
Ymax != Ymin	2 colors	Ymax	Ymin	Rmax	Rmin	Bmax	Bmin	P bits	6 Bytes
		6 bits	6 bits	5 bits	5 bits	5 bits	5 bits	16 bits	
Ymax != Ymin	>2 colors	Ymin	Ymax	Rmax	Rmin	Bmax	Bmin	P bits	8 Bytes
		6 bits	6 bits	5 bits	5 bits	5 bits	5 bits	32 bits	

Fig. 18

Ymax = Ymin	Amax = Amin = 0x00	1 color	Ymax	Ymax	Rmax	Bmax	00					3 Bytes
			6 bits	6 bits	5 bits	5 bits	2 bits					
Ymax = Ymin	Amax = Amin = 0xFF	1 color	Ymax	Ymax	Rmax	Bmax	11					3 Bytes
			6 bits	6 bits	5 bits	5 bits	2 bits					
Ymax = Ymin	Amax = Amin != 00 or FF	1 color	Ymax	Ymax	Rmax	Bmax	01	Amax	Amin			4/5 Bytes
			6 bits	6 bits	5 bits	5 bits	2 bits	4/8 bits	4/8 bits			
Ymax = Ymin	Amax != Amin	1 color	Ymax	Ymax	Rmax	Bmax	01	Amax	Amin	P bits		6/7 Bytes
		2 Alphas	6 bits	6 bits	5 bits	5 bits	2 bits	4/8 bits	4/8 bits	16 bits		
Ymax = Ymin	Amax != Amin	1 color	Ymax	Ymax	Rmax	Bmax	10	Amax	Amin	P bits		8/9 Bytes
		>2 Alphas	6 bits	6 bits	5 bits	5 bits	2 bits	4/8 bits	4/8 bits	32 bits		
Ymax != Ymin	X	2 colors	Ymax	Ymin	Rmax	Rmin	Bmax	Bmin	Amax	Amin	P bits	7/8 Bytes
			6 bits	6 bits	5 bits	5 bits	5 bits	5 bits	4/8 bits	4/8 bits	16 bits	
Ymax != Ymin	X	>2 colors	Ymin	Ymax	Rmax	Rmin	Bmax	Bmin	Amax	Amin	P bits	9/10 Bytes
			6 bits	6 bits	5 bits	5 bits	5 bits	5 bits	4/8 bits	4/8 bits	32 bits	

Fig. 19

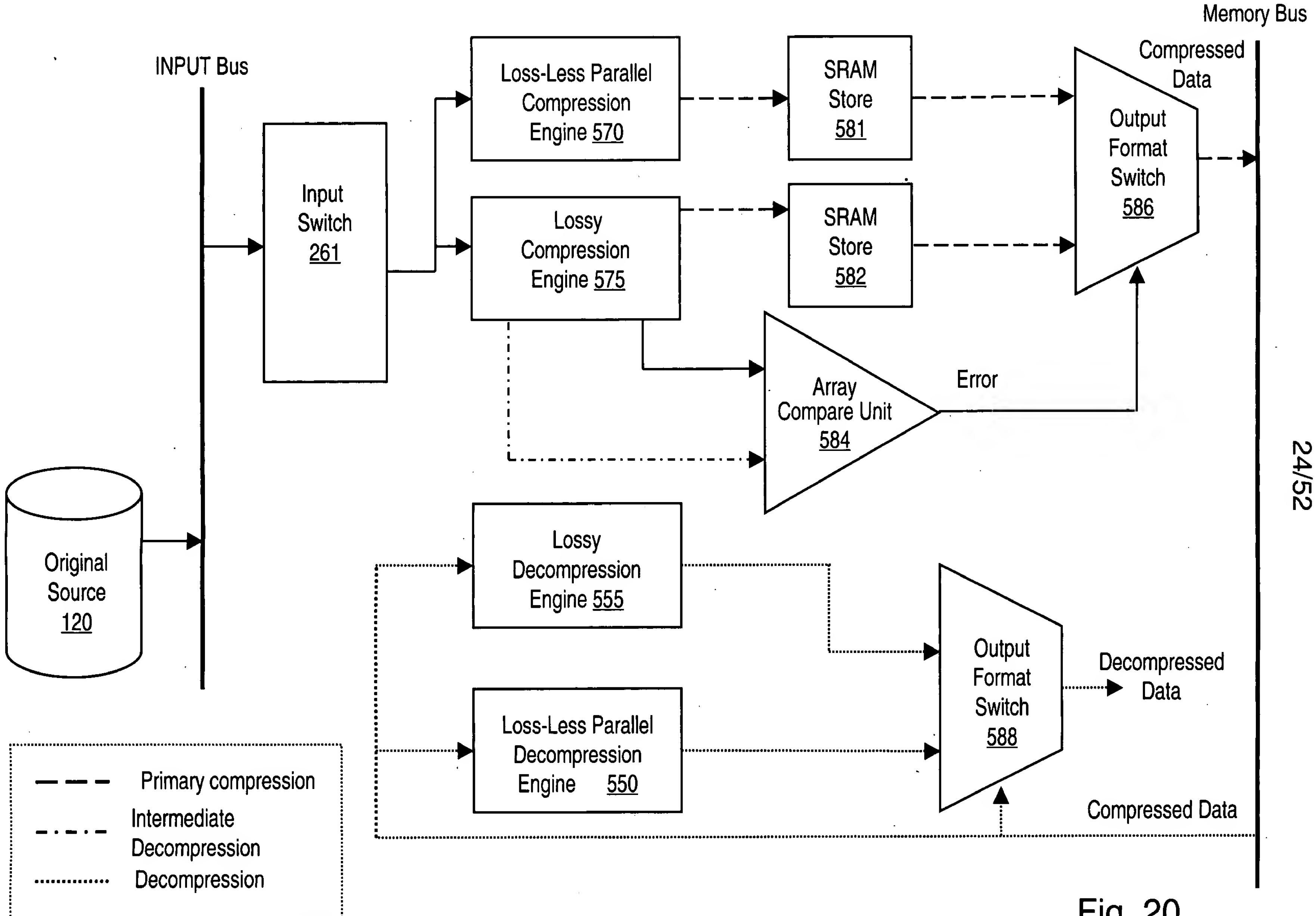


Fig. 20

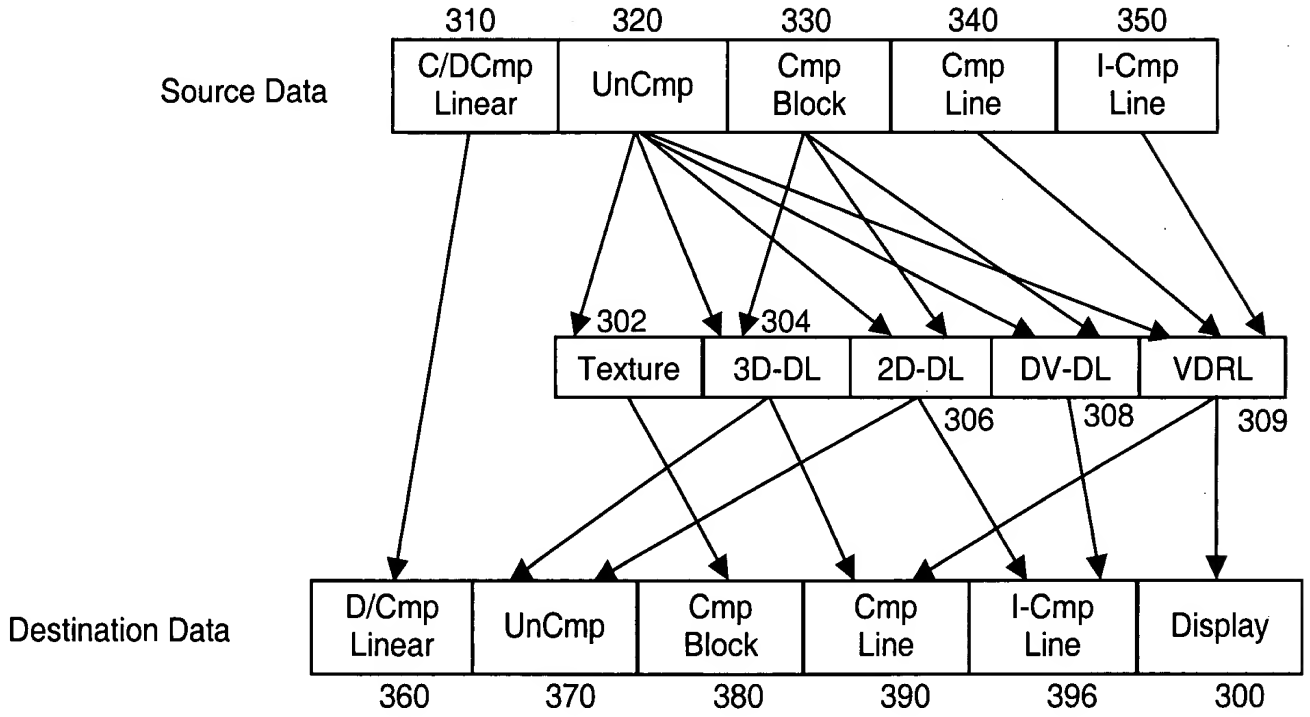

310
320
330
340
350
Source Data
C/DCmp Linear
UnCmp
Cmp Block
Cmp Line
I-Cmp Line
302
304
Texture
3D-DL
2D-DL
DV-DL
VDRL
306
308
309
Destination Data
D/Cmp Linear
UnCmp
Cmp Block
Cmp Line
I-Cmp Line
Display
360
370
380
390
396
300

Fig. 21

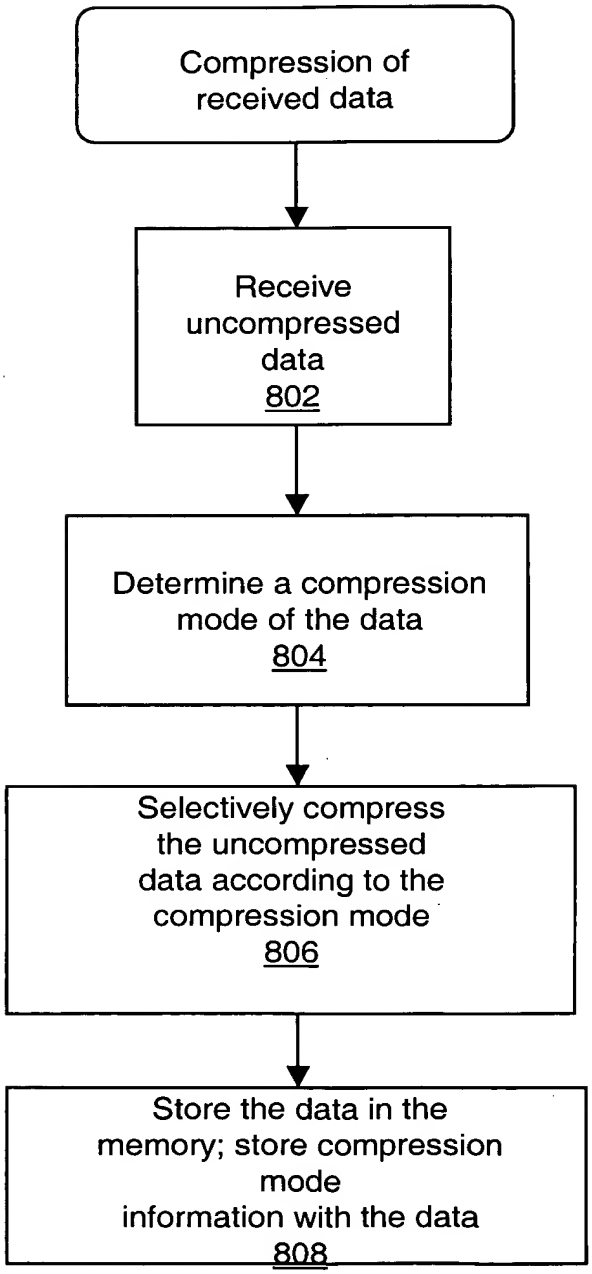

Compression of received data
Receive uncompressed data 802
Determine a compression mode of the data 804
Selectively compress the uncompressed data according to the compression mode 806
Store the data in the memory; store compression mode information with the data 808

Fig. 22

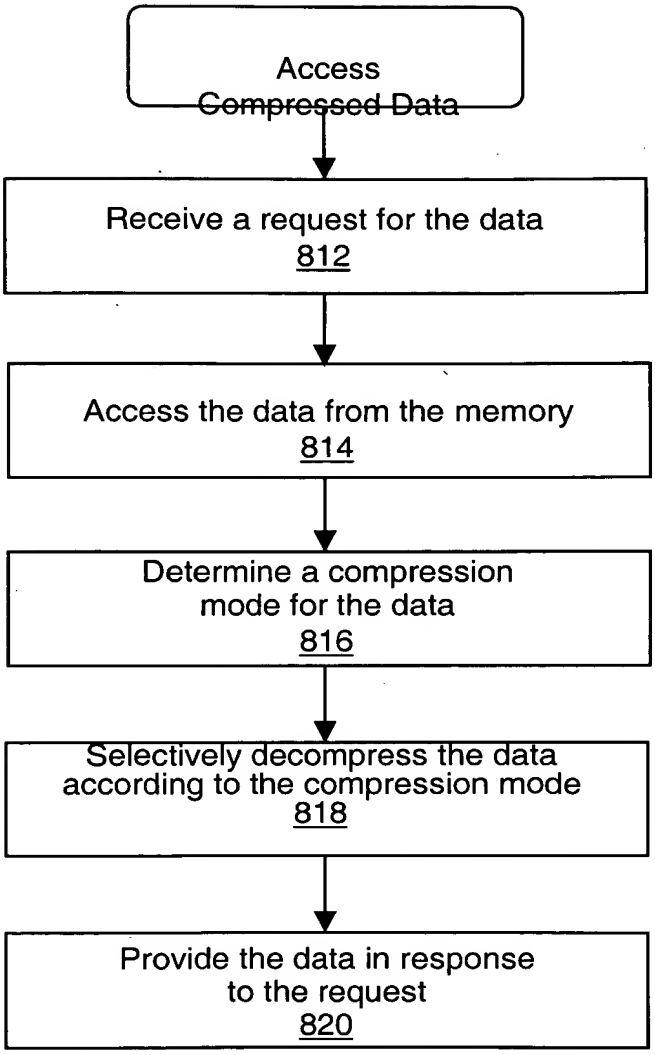

Access Compressed Data
Receive a request for the data
812
Access the data from the memory
814
Determine a compression mode for the data
816
Selectively decompress the data according to the compression mode
818
Provide the data in response to the request
820

Fig. 23

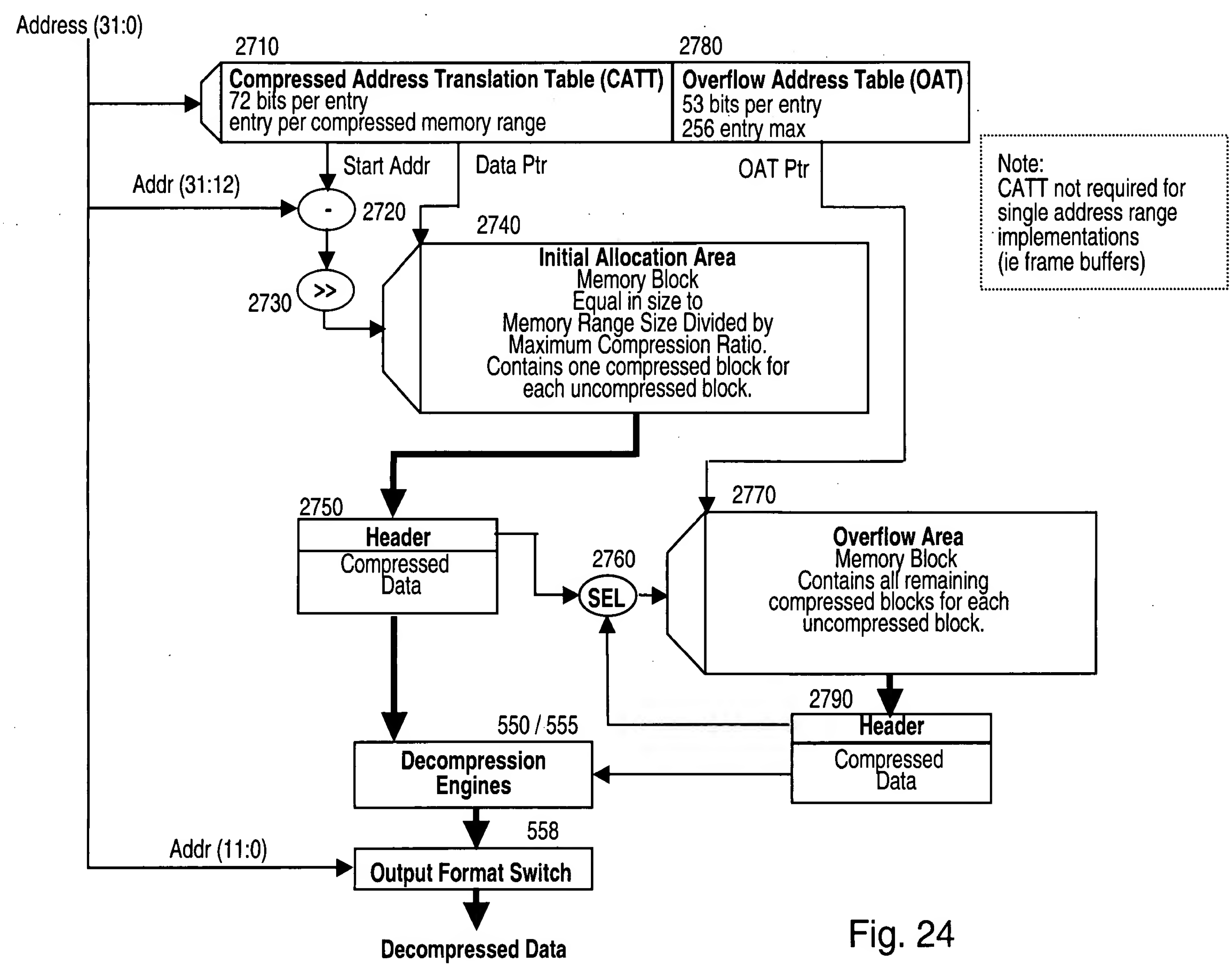

Address (31:0)
2710
Compressed Address Translation Table (CATT)
72 bits per entry
entry per compressed memory range
2780
Overflow Address Table (OAT)
53 bits per entry
256 entry max
Start Addr
Data Ptr
OAT Ptr
Addr (31:12)
-
2720
>>
2730
2740
Initial Allocation Area
Memory Block
Equal in size to
Memory Range Size Divided by
Maximum Compression Ratio.
Contains one compressed block for
each uncompressed block.
2750
Header
Compressed Data
2760
SEL
2770
Overflow Area
Memory Block
Contains all remaining
compressed blocks for each
uncompressed block.
2790
Header
Compressed Data
550 / 555
Decompression Engines
558
Addr (11:0)
Output Format Switch
Decompressed Data
Note:
CATT not required for
single address range
implementations
(ie frame buffers)

Fig. 24

Memory Allocation Fields

Compressed Address Translation Table (CATT) – 128 Entry Design Limit				
Starting Addr	Ending Addr	Type	Data Ptr	OAT Ptr
20 bits	20 bits	4 bits	20 bits	8 bits
4GB Addressability		Compressed		
4K Boundry	4K Boundry	Blk Size	4K Boundry	4K Boundry

Overflow Address Table (OAT) – 256 Entry Max			
Overflow Ptr	Next Block Ptr	Next OAT Ptr	Next OAT Valid
20 bits	24 bits	8 bits	1 bit
4 GB Addressability		Points to next entry	
4K Boundry		in this table	

Initial Header Description		
Value	# of bits	Meaning
0	1	Last Block/Unused
10 A (20 bits)	22	The next block is at offset A in the Overflow Area
11 IA(8+20 bits)	30	The next block is at offset A in the Overflow Area of OAT entry I

Overflow Header Description		
Value	# of bits	Meaning
00	2	Last Block/Unused
01	2	The next block follows physically after this one
10A (8 bits)	10	The next block is A blocks before this one (or after?)
110A (20 bits)	23	The next block is at offset A in the Overflow Area
111 IA (8+20 bits)	31	The next block is at offset A in the Overflow Area of OAT entry I

Fig. 25

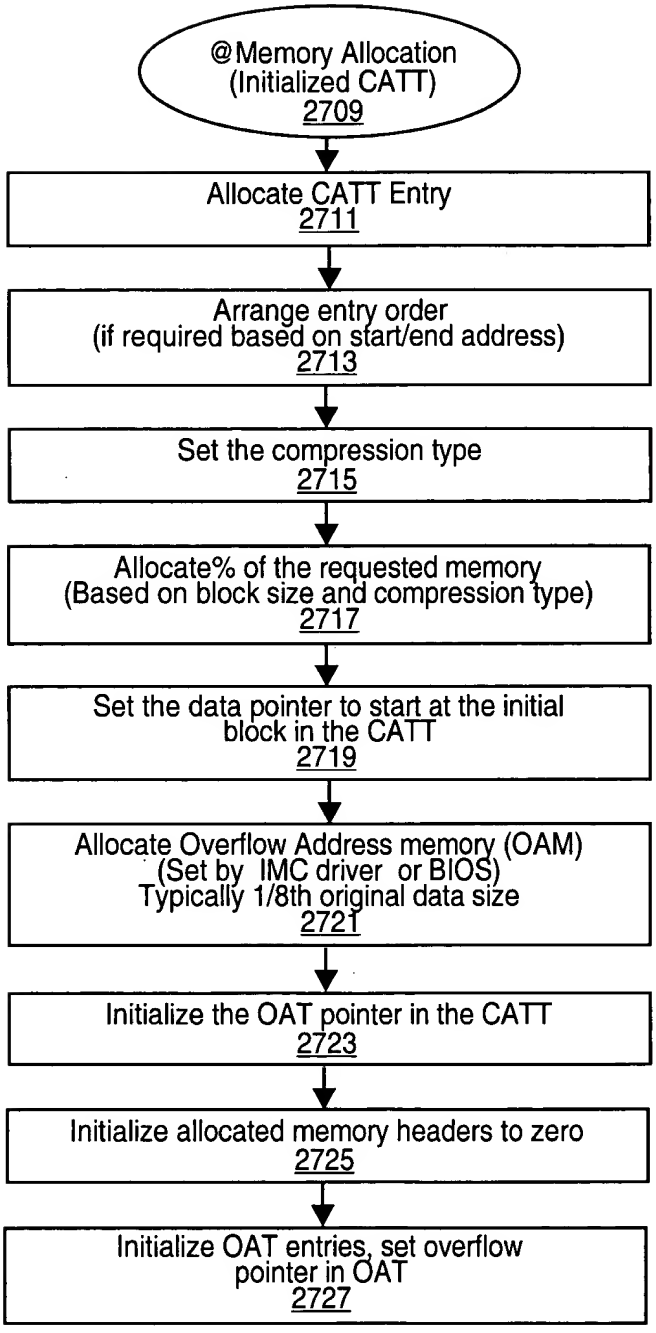

@Memory Allocation
(Initialized CATT)
2709
Allocate CATT Entry
2711
Arrange entry order
(if required based on start/end address)
2713
Set the compression type
2715
Allocate% of the requested memory
(Based on block size and compression type)
2717
Set the data pointer to start at the initial
block in the CATT
2719
Allocate Overflow Address memory (OAM)
(Set by IMC driver or BIOS)
Typically 1/8th original data size
2721
Initialize the OAT pointer in the CATT
2723
Initialize allocated memory headers to zero
2725
Initialize OAT entries, set overflow
pointer in OAT
2727

Fig. 26

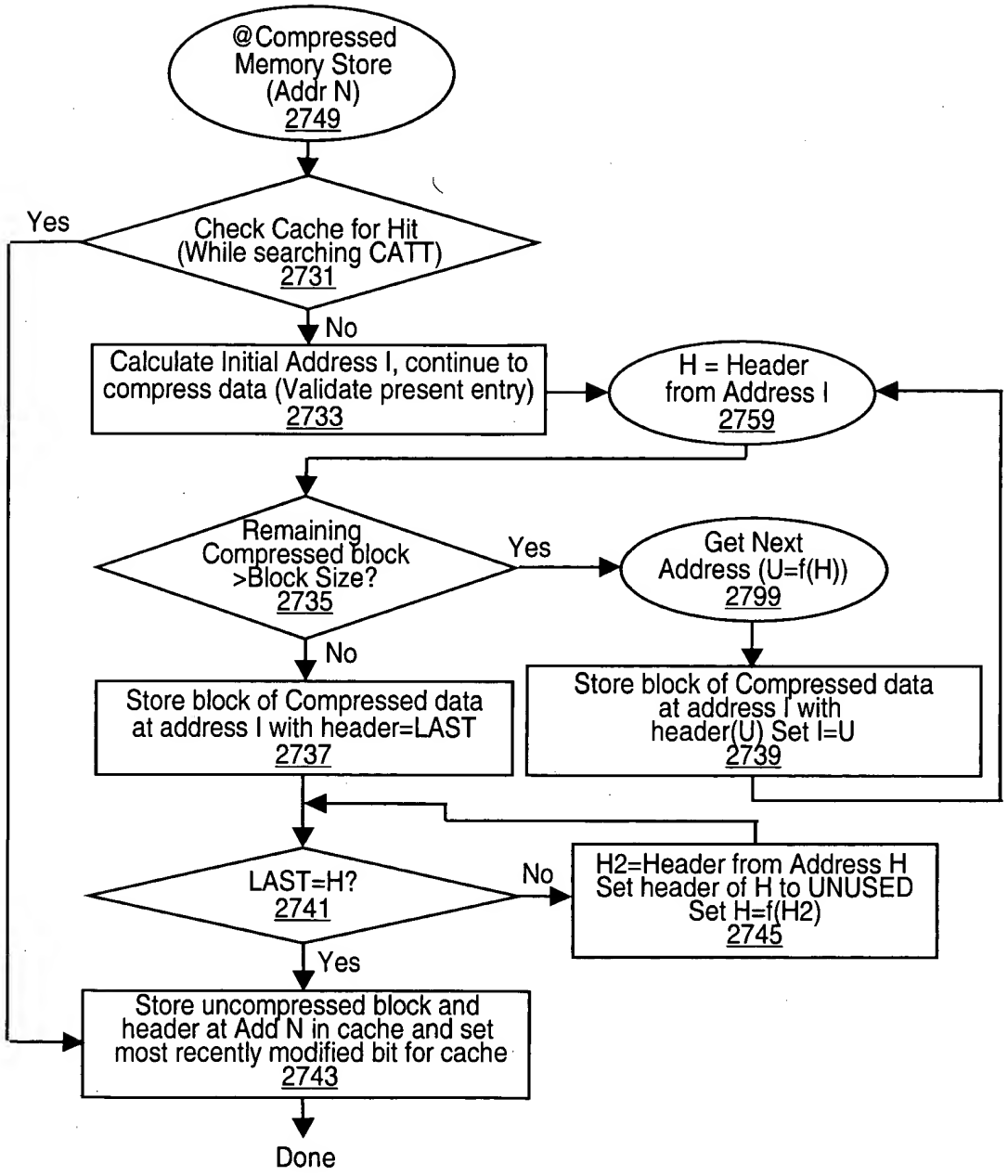

@Compressed Memory Store (Addr N) 2749
Check Cache for Hit (While searching CATT) 2731
Yes
No
Calculate Initial Address I, continue to compress data (Validate present entry) 2733
H = Header from Address I 2759
Remaining Compressed block >Block Size? 2735
Yes
Get Next Address (U=f(H)) 2799
No
Store block of Compressed data at address I with header=LAST 2737
Store block of Compressed data at address I with header(U) Set I=U 2739
LAST=H? 2741
No
H2=Header from Address H Set header of H to UNUSED Set H=f(H2) 2745
Yes
Store uncompressed block and header at Add N in cache and set most recently modified bit for cache 2743
Done

Fig. 27

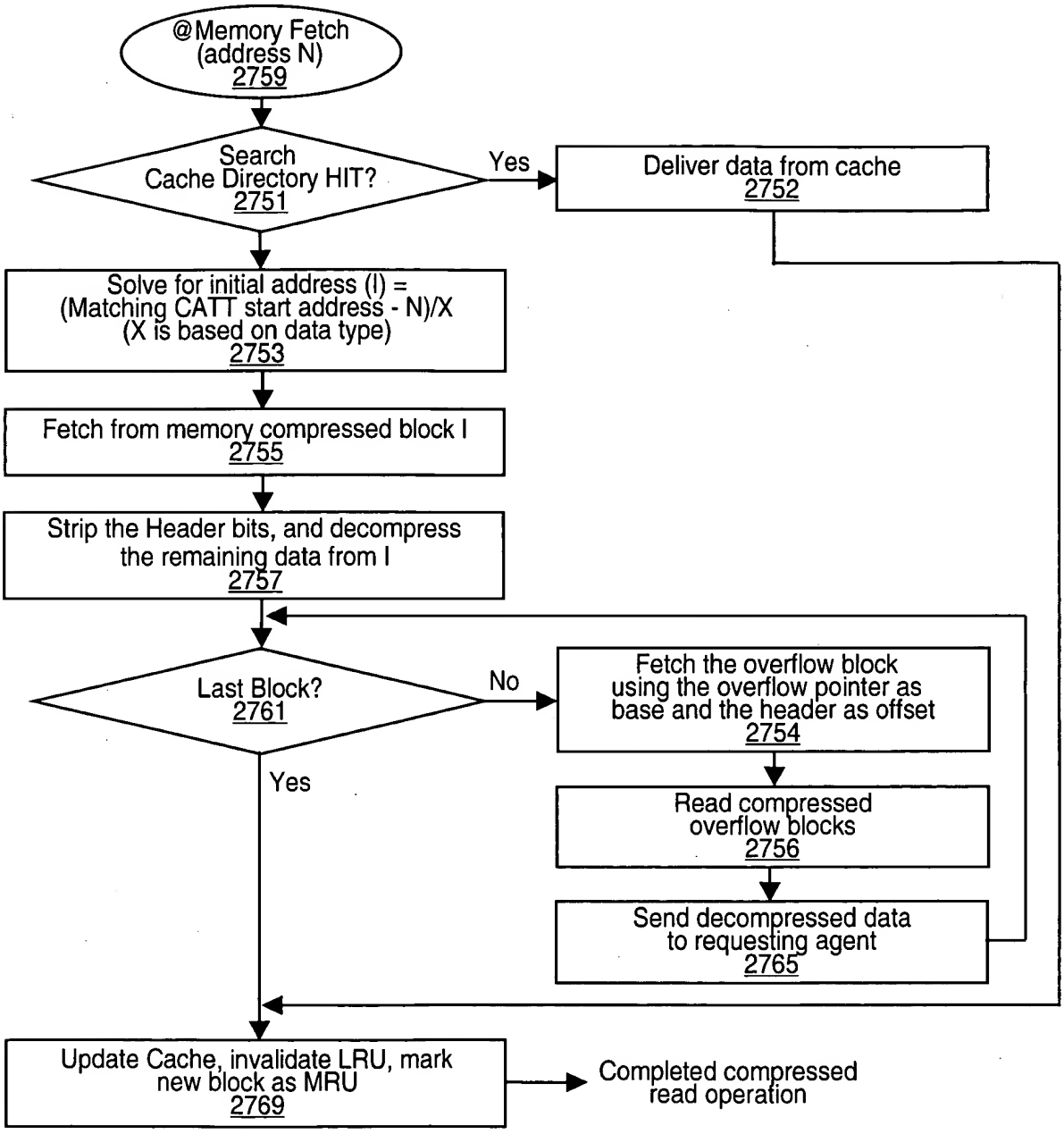

@Memory Fetch
(address N)
2759
Search
Cache Directory HIT?
2751
Yes
Deliver data from cache
2752
Solve for initial address (I) =
(Matching CATT start address - N)/X
(X is based on data type)
2753
Fetch from memory compressed block I
2755
Strip the Header bits, and decompress
the remaining data from I
2757
Last Block?
2761
No
Fetch the overflow block
using the overflow pointer as
base and the header as offset
2754
Yes
Read compressed
overflow blocks
2756
Send decompressed data
to requesting agent
2765
Update Cache, invalidate LRU, mark
new block as MRU
2769
Completed compressed
read operation

Fig. 28

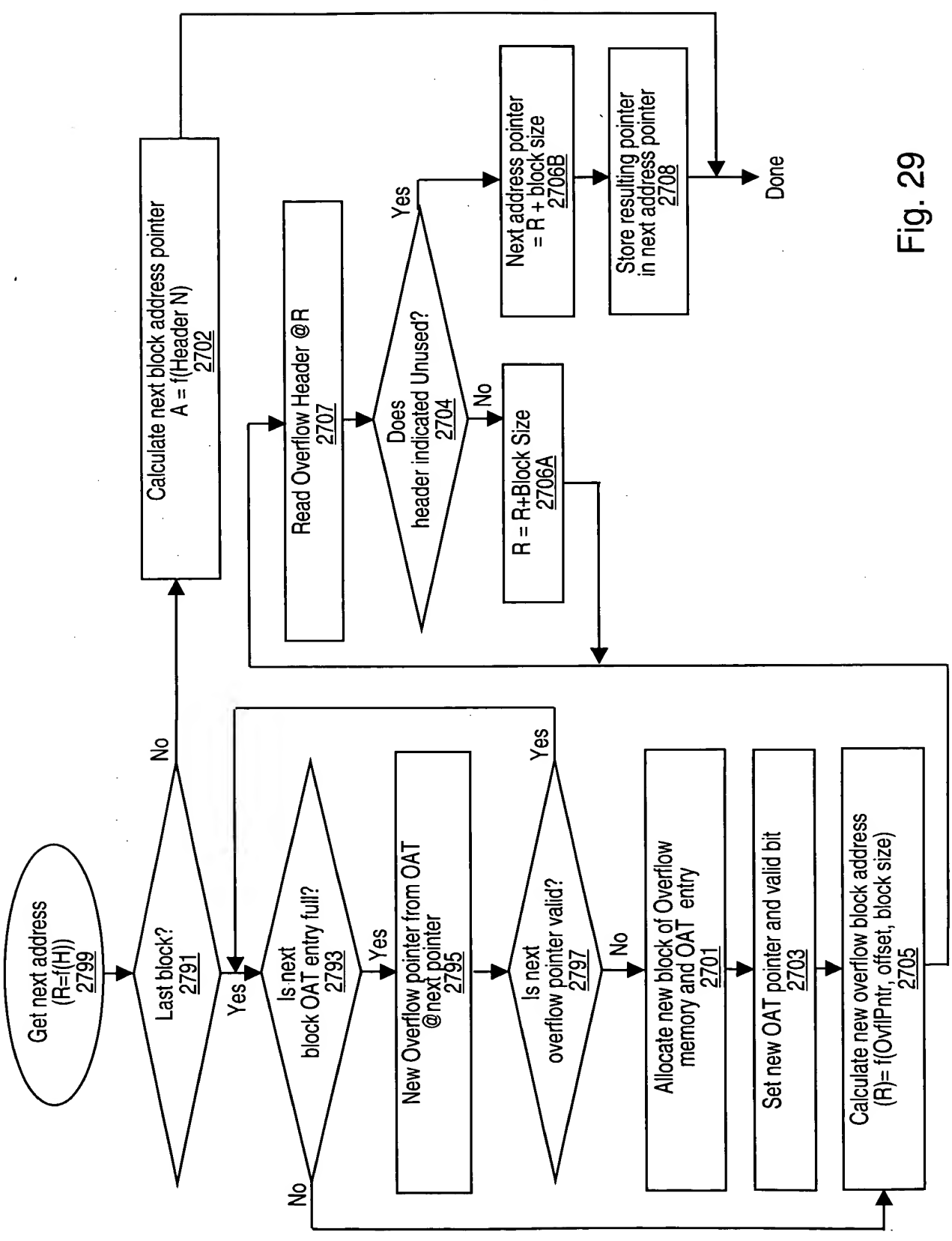
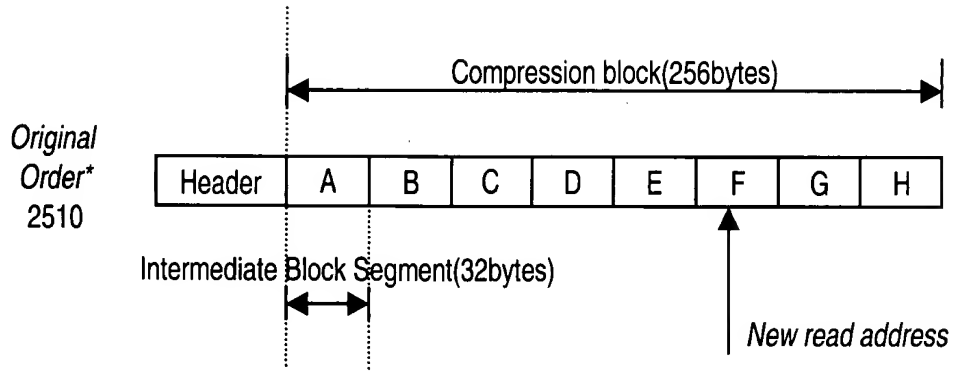

Get next address (R=f(H)) 2799
Last block? 2791
No
Yes
Calculate next block address pointer A = f(Header N) 2702
Is next block OAT entry full? 2793
Yes
No
Read Overflow Header @R 2707
Does header indicated Unused? 2704
Yes
No
Next address pointer = R + block size 2706B
Store resulting pointer in next address pointer 2708
Done
R = R+Block Size 2706A
New Overflow pointer from OAT @next pointer 2795
Is next overflow pointer valid? 2797
Yes
No
Allocate new block of Overflow memory and OAT entry 2701
Set new OAT pointer and valid bit 2703
Calculate new overflow block address (R)= f(OvflPntr, offset, block size) 2705

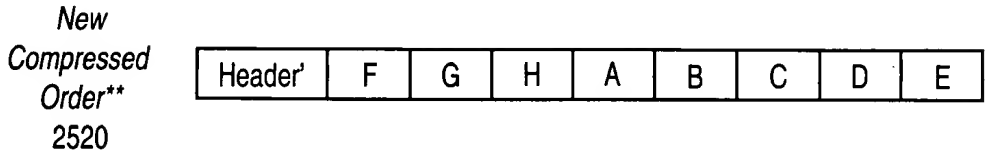
Fig. 29

Uncomp Block Bytes	Type	Initial Block Size Bytes	Overflow Block Size Bytes	Max Comp Ratio (X:1)	Initial Allocation	Header w/o OF	Header w/ OF Non-Frag	Header w/ OF Fragmented
4096	8	256	64	16	6%	0.0%	0.4%	4.1%
2048	7	128	64	16	6%	0.1%	0.5%	4.2%
1024	6	64	64	16	6%	0.2%	0.6%	4.3%
512	5	64	64	8	13%	0.2%	0.9%	4.3%
256	4	64	64	4	25%	0.2%	1.4%	4.3%
128	3	32	32	4	25%	0.4%	2.8%	8.8%
64	2	32	16	2	50%	0.4%	5.1%	13.6%
32	1	32	8	1	100%	0.4%	8.9%	11.5%

Fig. 30



* Header tag field is '0' indicating in original order



** Header tag field is '5' indicating out of order

2530

1) Read compressed block from memory
2) Decompress to L3 data cache
3) Store Position tag (@F) in table
4) Re-compress block out of order
5) Attach header with tag (@F)
6) Write compressed block back to memory

Fig. 31

Bytes Compressed	Flag	Index	Count	Data	**Bits Used**
0	0	-	-	8b	9
1	10	6b	-	-	8
2	1100	6b	-	-	10
3	1101	6b	-	-	10
4	1110	6b	-	-	10
5	1111000	6b	-	-	13
6	1111001	6b	-	-	13
7	1111010	6b	-	-	13
8	1111011	6b	-	-	13
9	1111100	6b	-	-	13
10	1111101	6b	-	-	13
11	1111110	6b	-	-	13
>11	1111111	6b	12b	-	25

Fig. 32

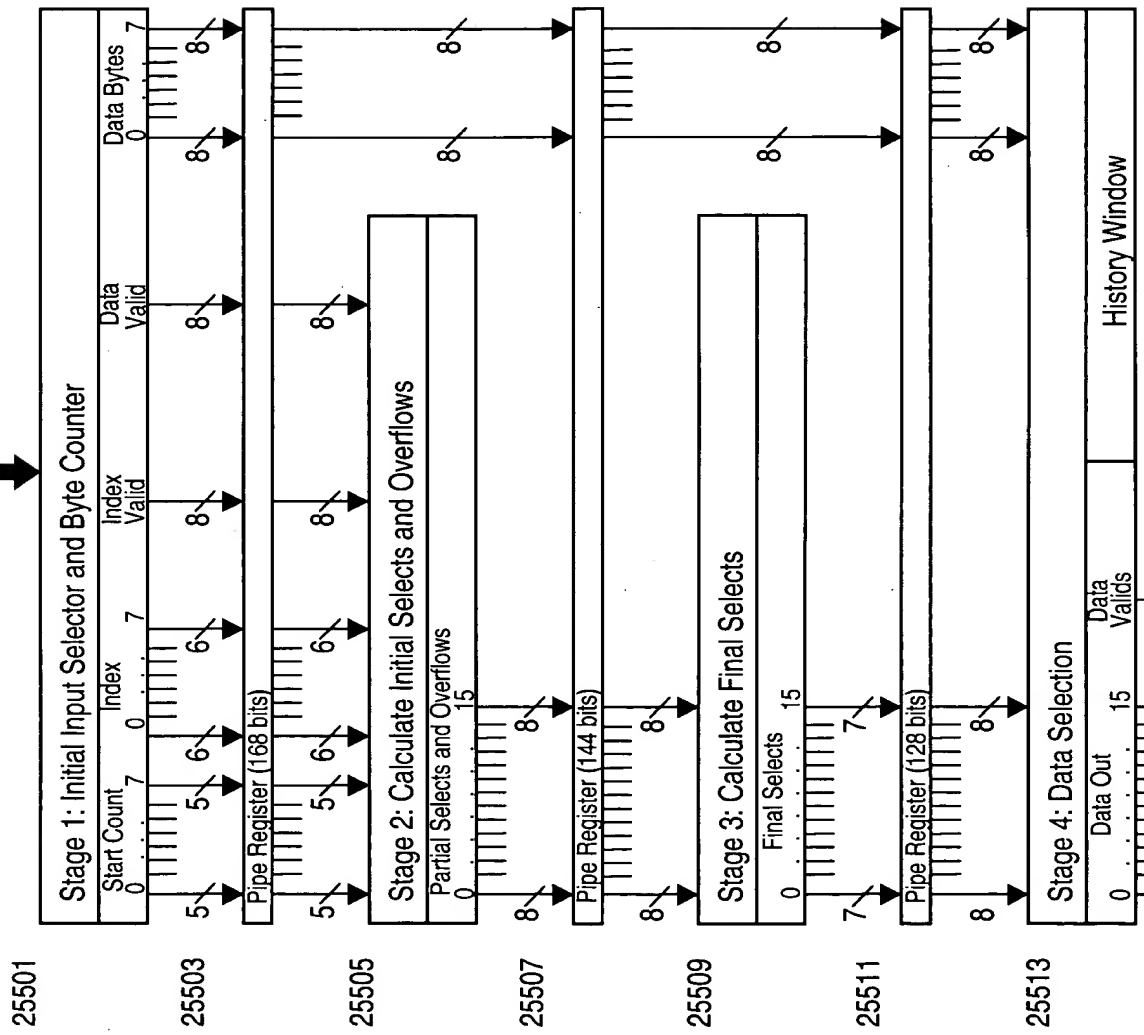

Input Data 8 Bytes
Stage 1: Initial Input Selector and Byte Counter
Start Count
Index
Index Valid
Data Valid
Data Bytes
Pipe Register (168 bits)
Stage 2: Calculate Initial Selects and Overflows
Partial Selects and Overflows
Pipe Register (144 bits)
Stage 3: Calculate Final Selects
Final Selects
Pipe Register (128 bits)
Stage 4: Data Selection
Data Out
Data Valids
History Window
25501
25503
25505
25507
25509
25511
25513

Fig. 33

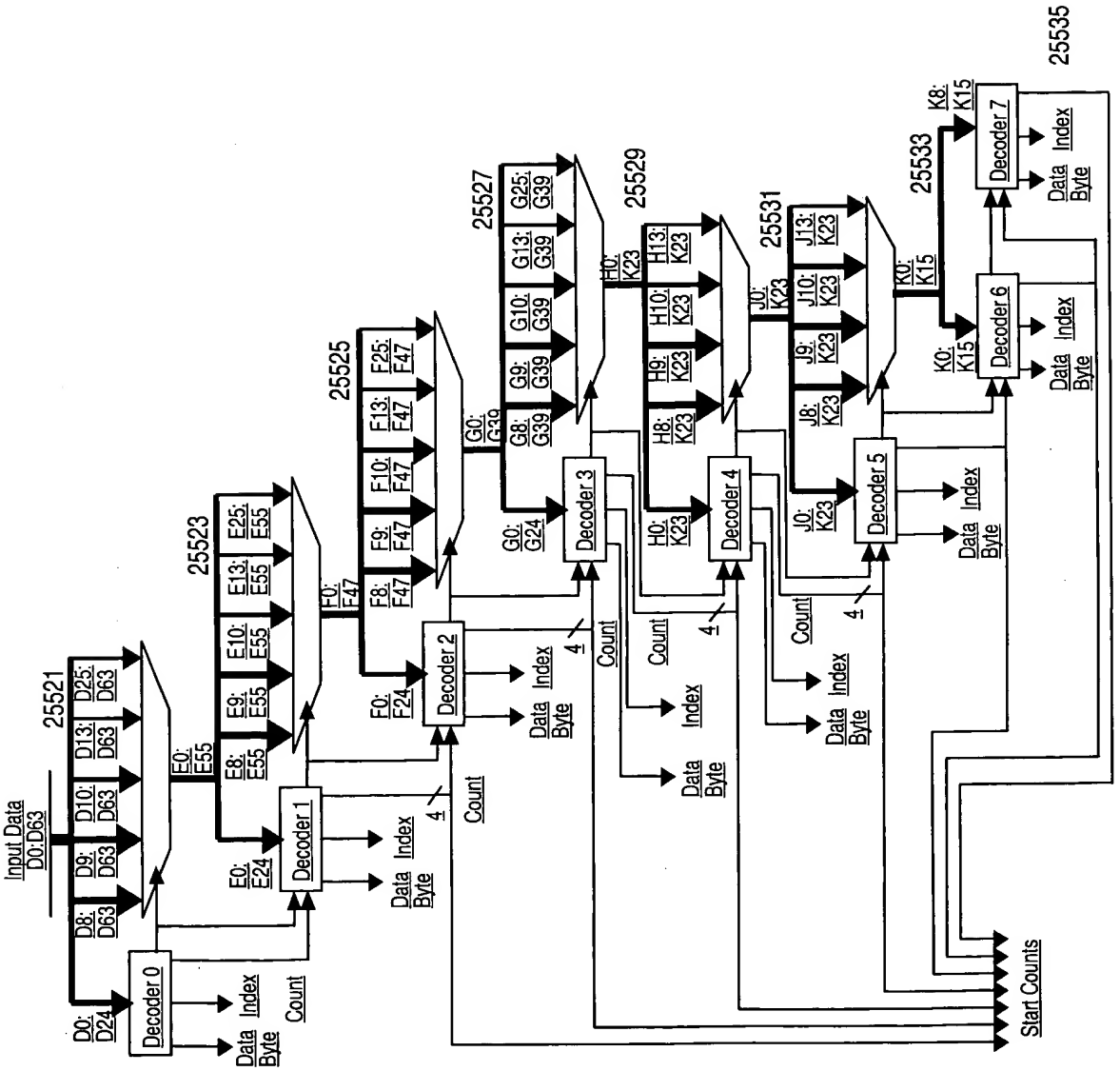

Input Data D0:D63
25521
D0: D24
D8: D63
D9: D63
D10: D63
D13: D63
D25: D63
Decoder 0
Data Byte
Index
Count
25523
E0: E24
E0: E55
E8: E55
E9: E55
E10: E55
E13: E55
E25: E55
Decoder 1
Data Byte
Index
Count
25525
F0: F24
F0: F47
F8: F47
F9: F47
F10: F47
F13: F47
F25: F47
Decoder 2
Data Byte
Index
Count
25527
G0: G24
G0: G38
G8: G39
G9: G39
G10: G39
G13: G39
G25: G39
Decoder 3
Data Byte
Index
Count
25529
H0: K23
H8: K23
H9: K23
H10: K23
H13: K23
Decoder 4
Data Byte
Index
Count
25531
J0: K23
J8: K23
J9: K23
J10: K23
J13: K23
Decoder 5
Data Byte
Index
Count
25533
K0: K15
K8: K15
Decoder 6
Data Byte
Index
25535
Decoder 7
Data Byte
Index
Start Counts

Fig. 34

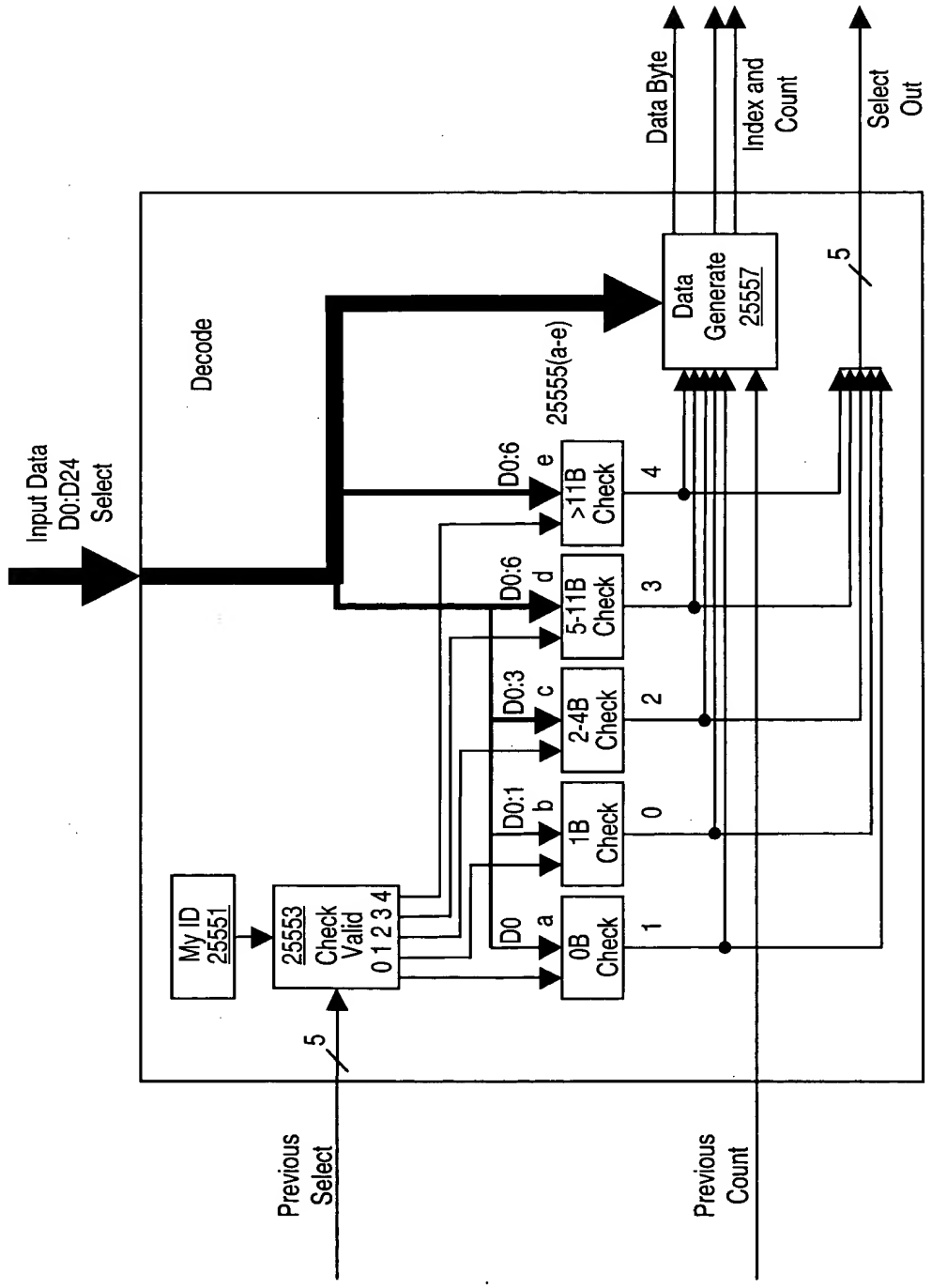

Input Data
D0:D24
Select
Decode
My ID
25551
25553
Check
Valid
0 1 2 3 4
5
Previous
Select
D0
a
0B
Check
1
D0:1
b
1B
Check
0
D0:3
c
2-4B
Check
2
D0:6
d
5-11B
Check
3
D0:6
e
>11B
Check
4
25555(a-e)
Data
Generate
25557
Data Byte
Index and
Count
Select
Out
5
Previous
Count

Fig. 35

Previous Select	10	08	04	02	01	00
My ID=01	1F	1F	1F	1F	1F	00
My ID=02	1F	1F	1F	1F	1F	00
My ID=04	1F	1F	1F	1F	1F	00
My ID=08	1F	1F	1F	1F	1E	00
My ID=10	1F	1F	1F	1F	1E	00
My ID=20	1E	1E	1E	1E	00	00
My ID=40	1E	1E	1E	1C	00	00
My ID=80	08	00	00	00	00	00

Fig. 36a

Select	10	08	04	02	01	00
Data Byte	X	D1:D8	X	X	X	X
Index	D2:D7	X	D4:D9	D7:D12	D7:D12	X
Count	PC+1	PC+1	D2:D3+PC+2	D4:D6+PC+5	D13:D24+PC	X

Fig. 36b

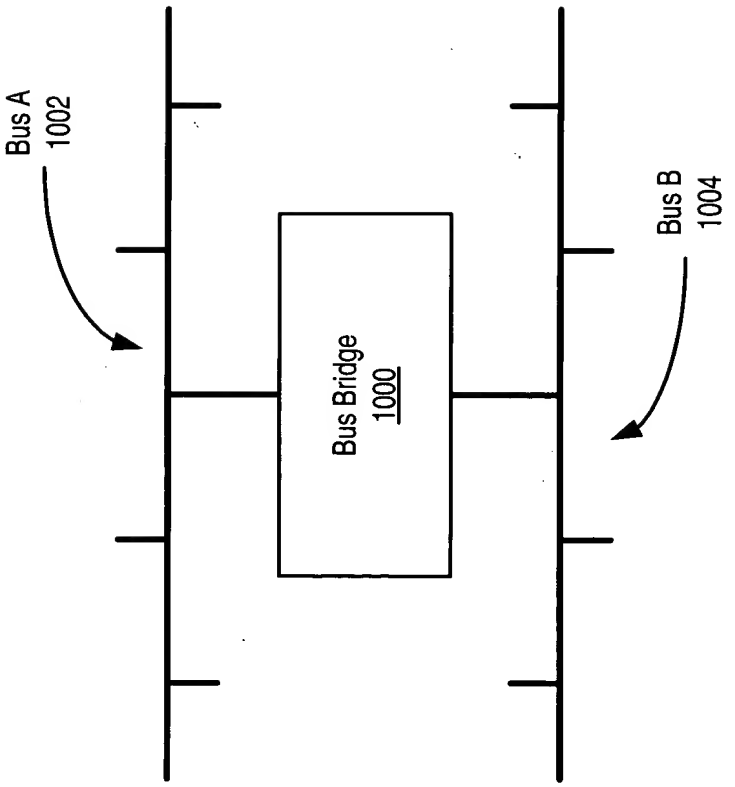


FIG. 37
Bus Bridge

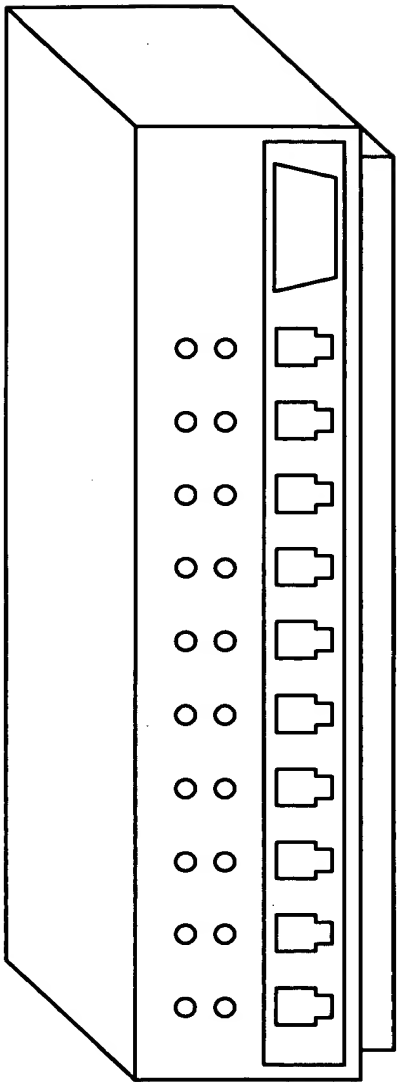


FIG. 38
Network Hub

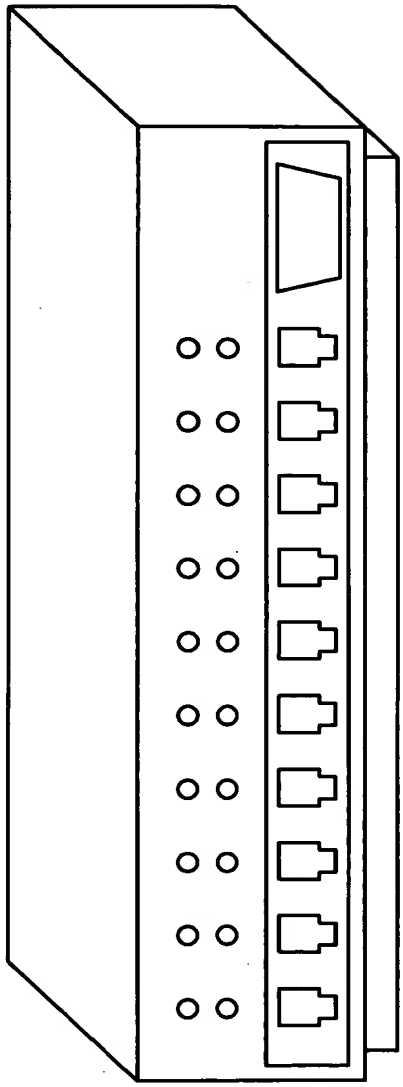


FIG. 39
Network Switch

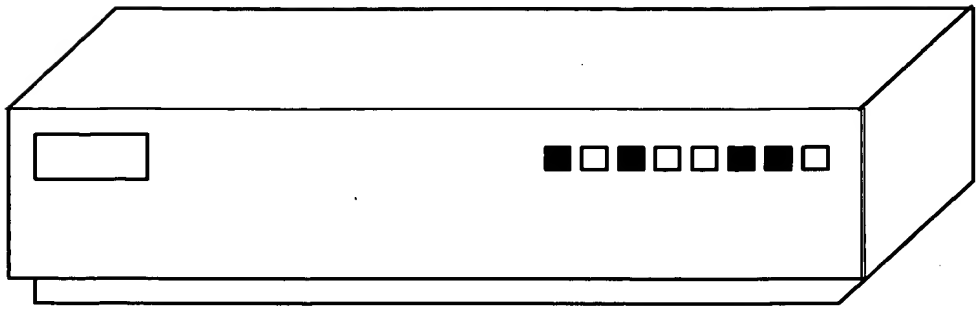


FIG. 40
Network Bridge

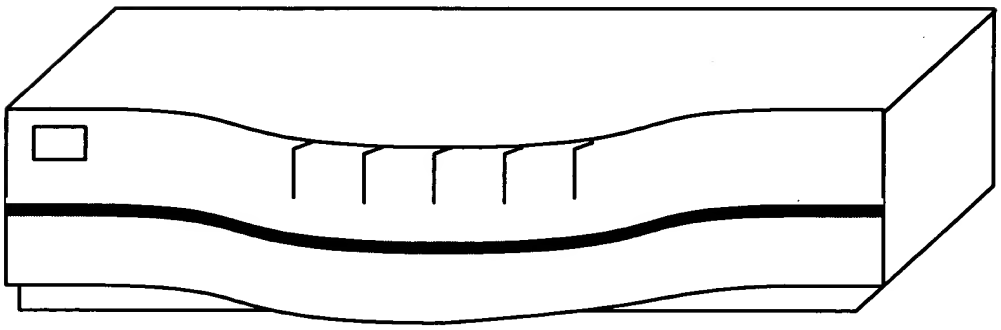


FIG.41
Network Router

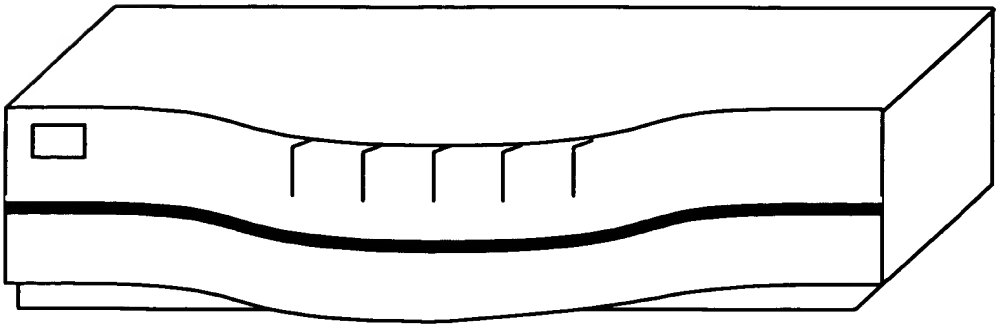


FIG. 42
Network Brouter

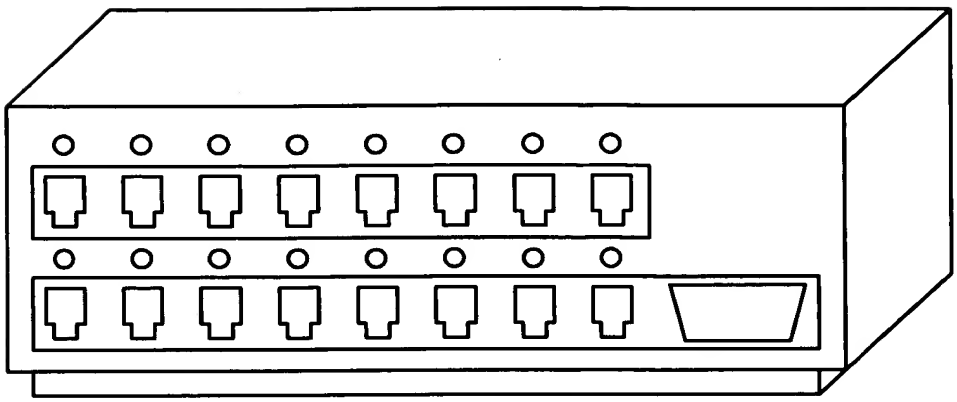


FIG. 43A
Multiplexer

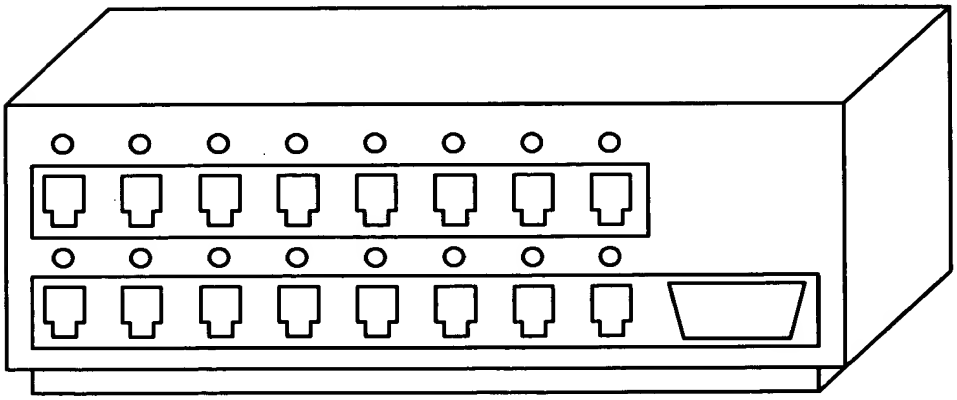


FIG. 43B
Demultiplexer

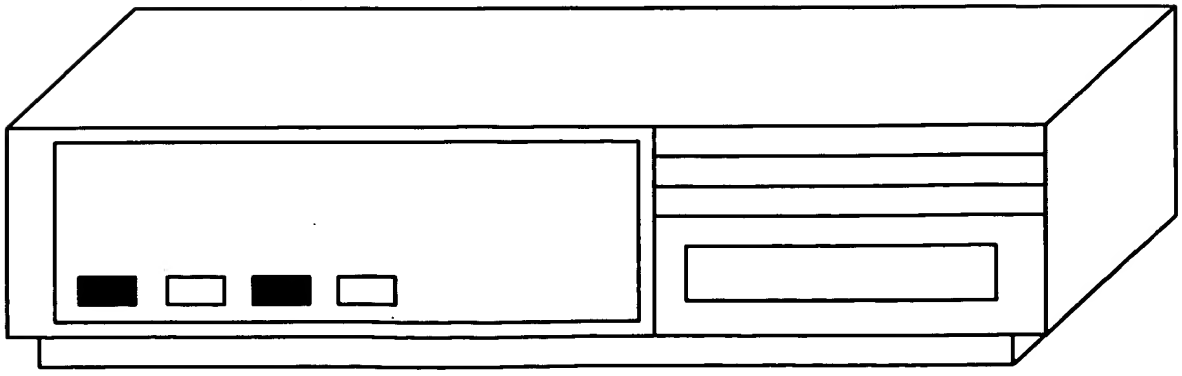


FIG. 44
Terminal Server

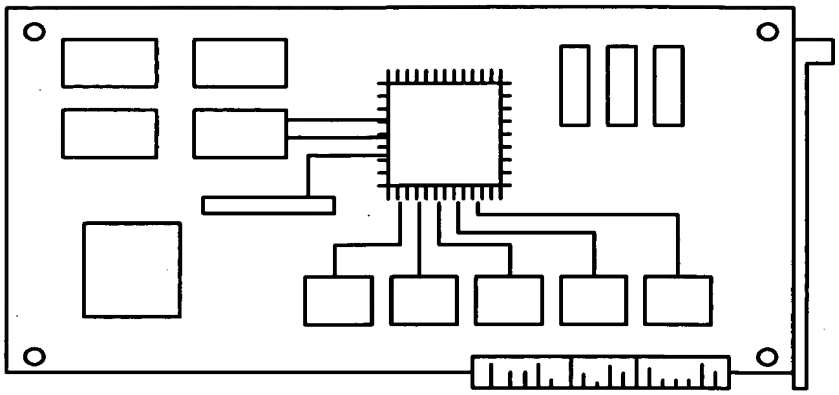


FIG. 45
Network Interface Card

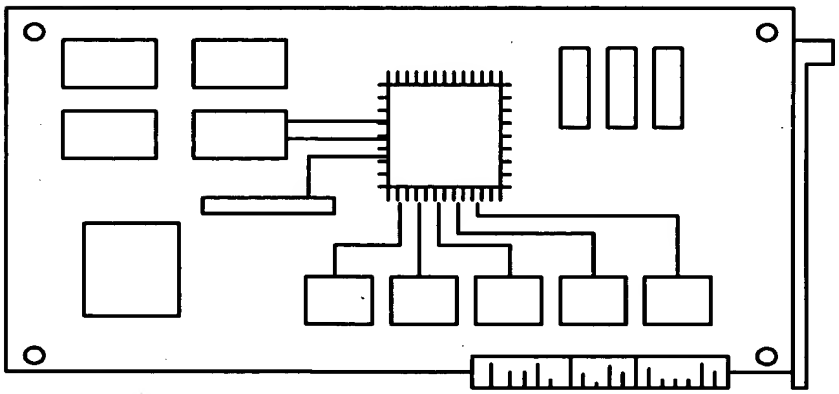


FIG. 46
ISDN adapter

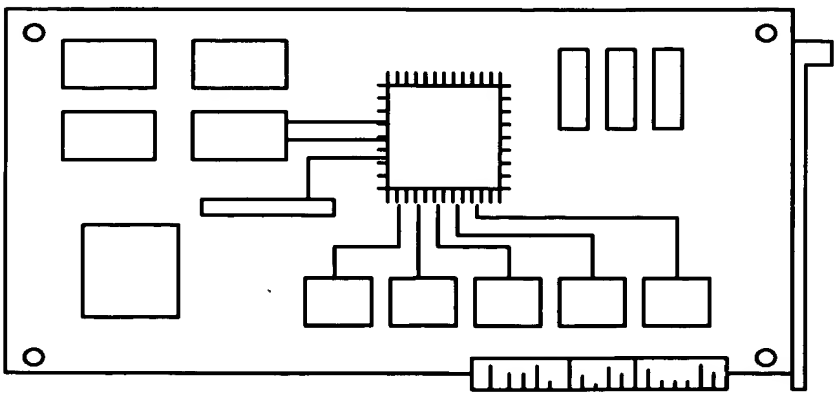


FIG. 47
ATM adapter

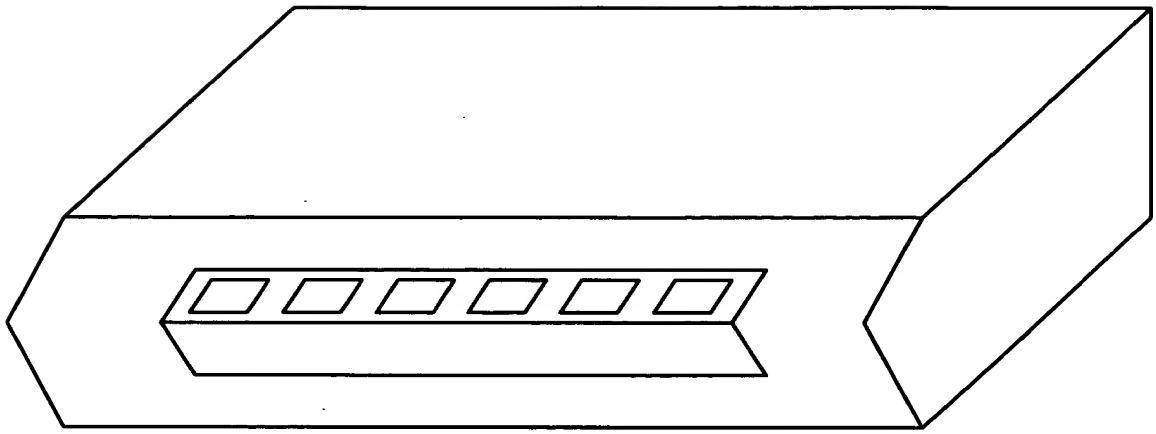


FIG. 48
Modem

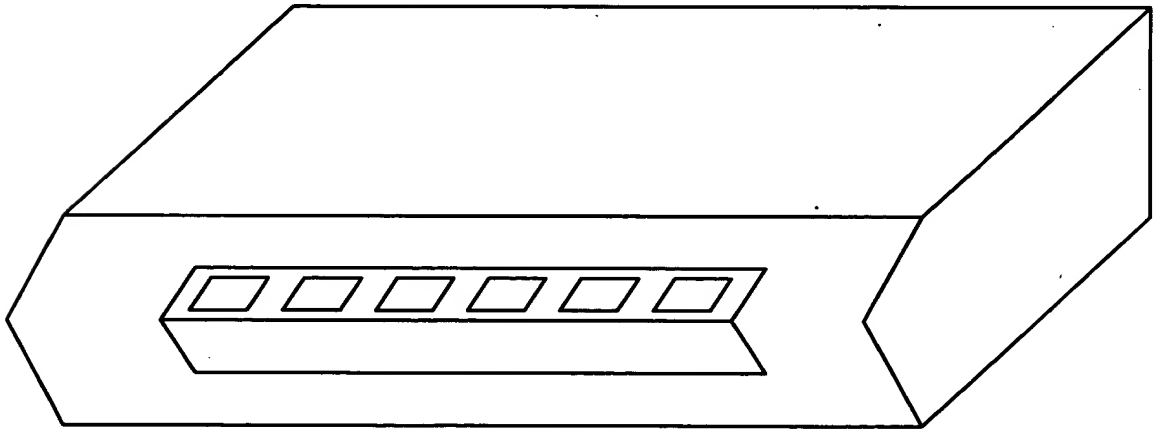


FIG. 49
Cable modem

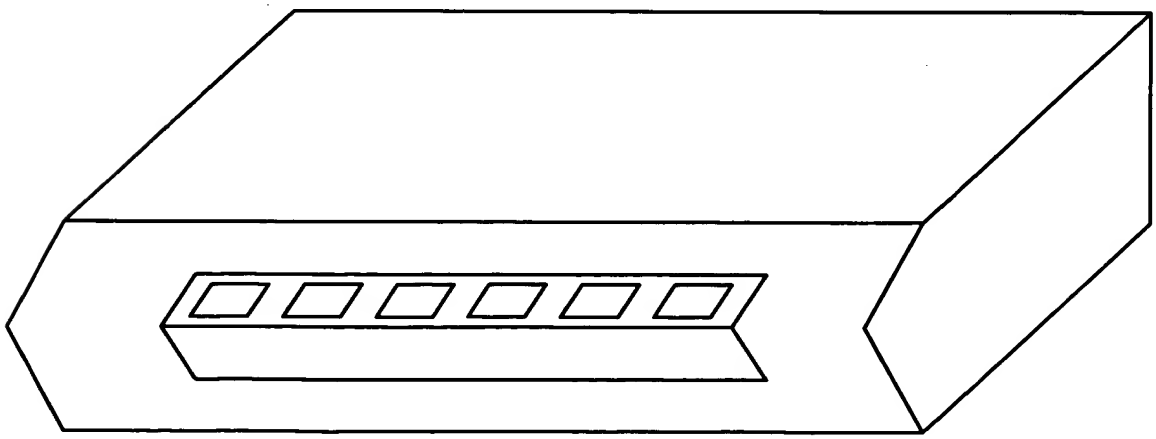


FIG. 50
DSL adapter

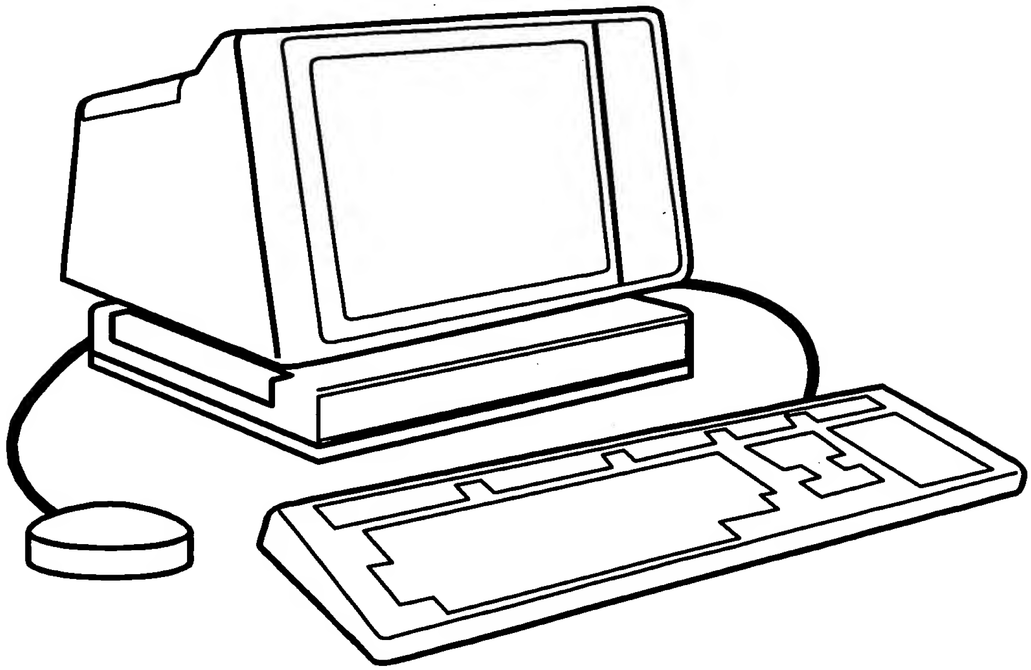


FIG. 52
Network appliance

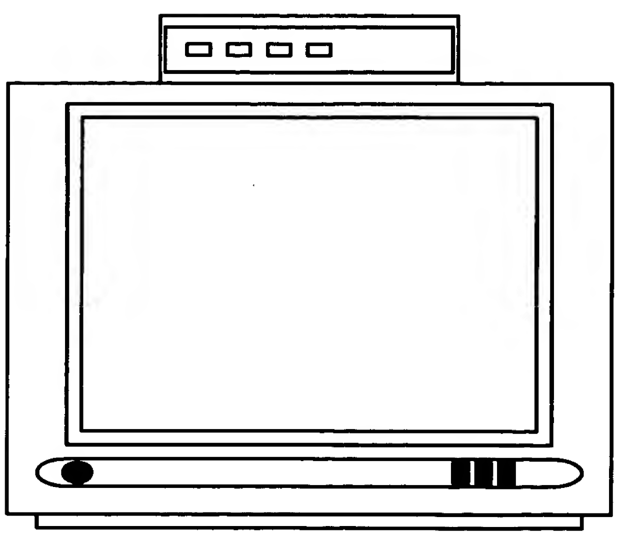


FIG. 52
Television set with set top box

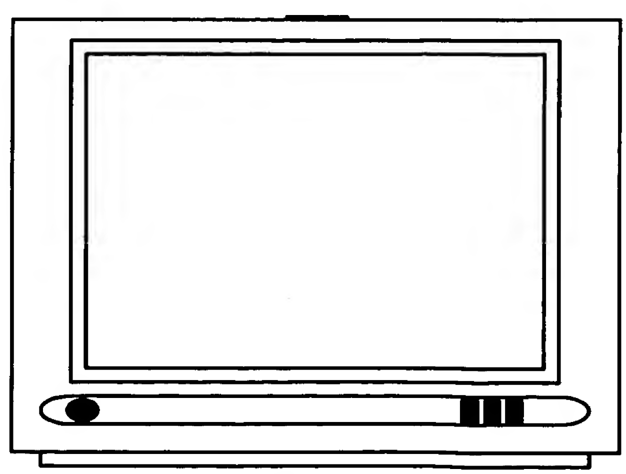


FIG. 53
HDTV set

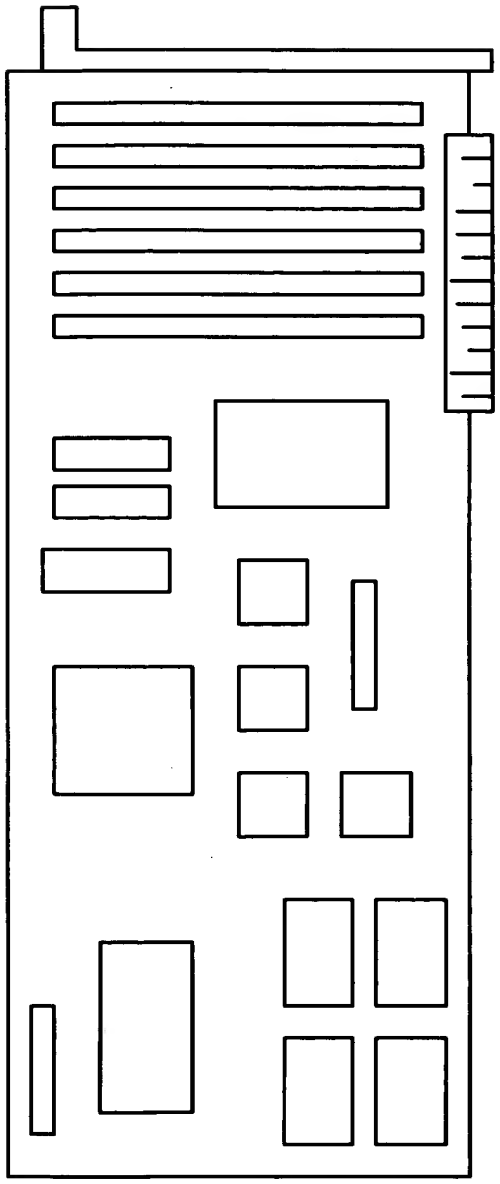


FIG. 54A
Digital-to-Analog Card (DAC)

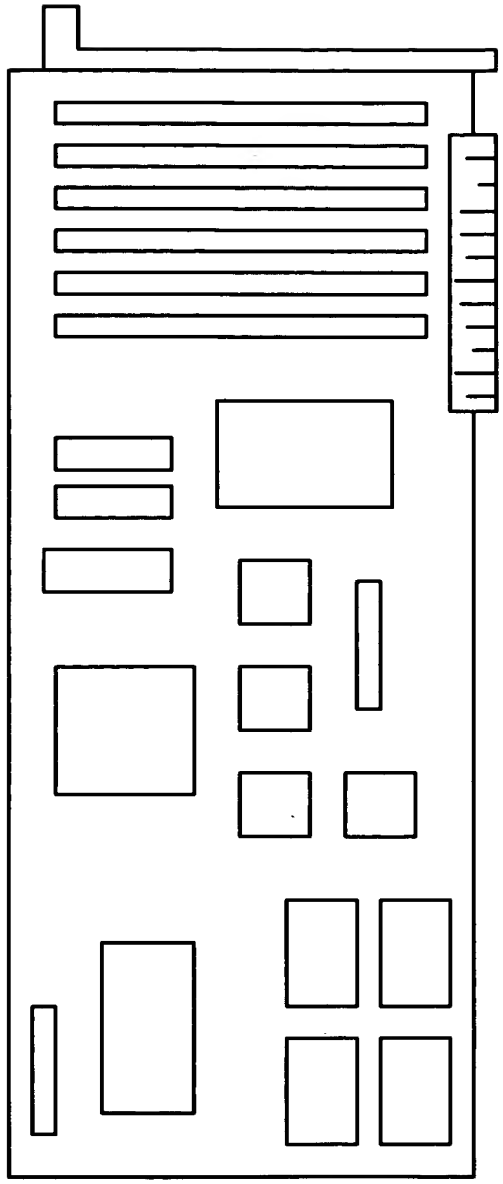


FIG. 54B
Analog-to Digital Card (ADC)

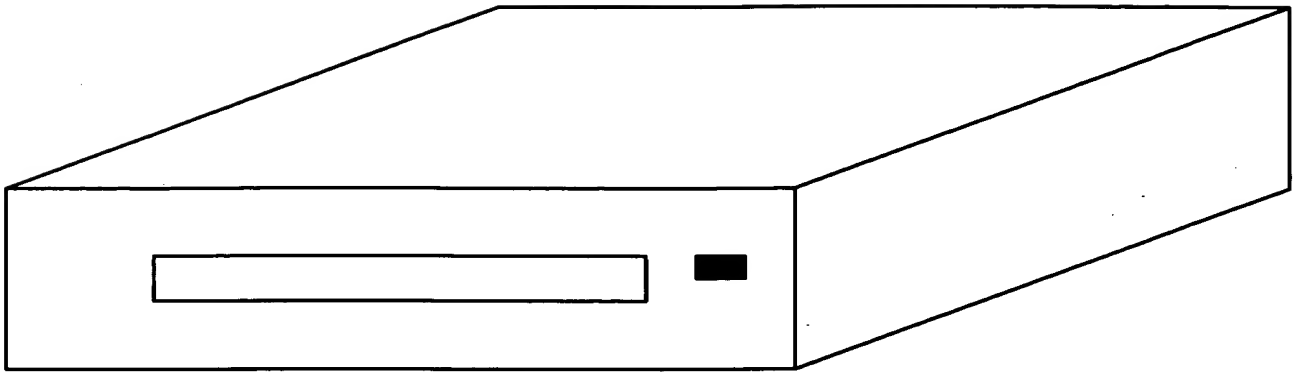


FIG. 55A
Compact Disk (CD) Reader Device

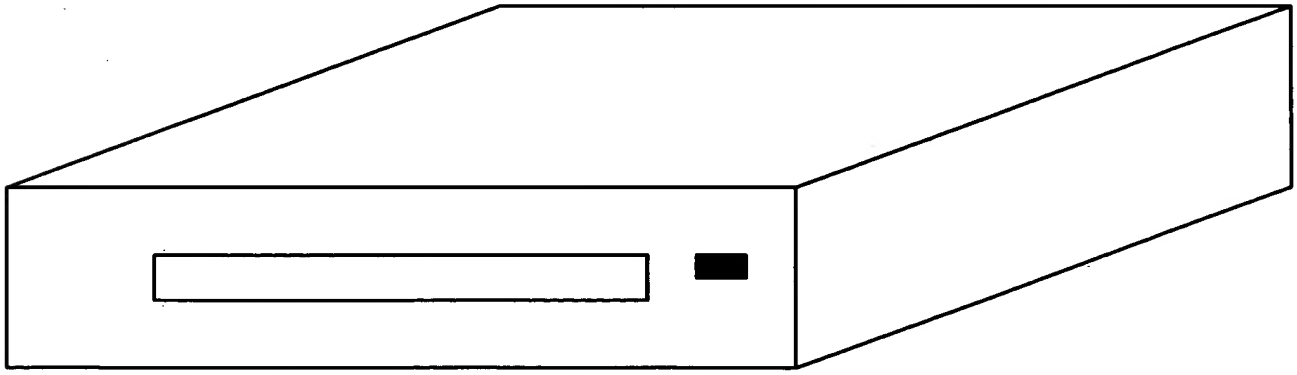


FIG. 55B
CD-R Device

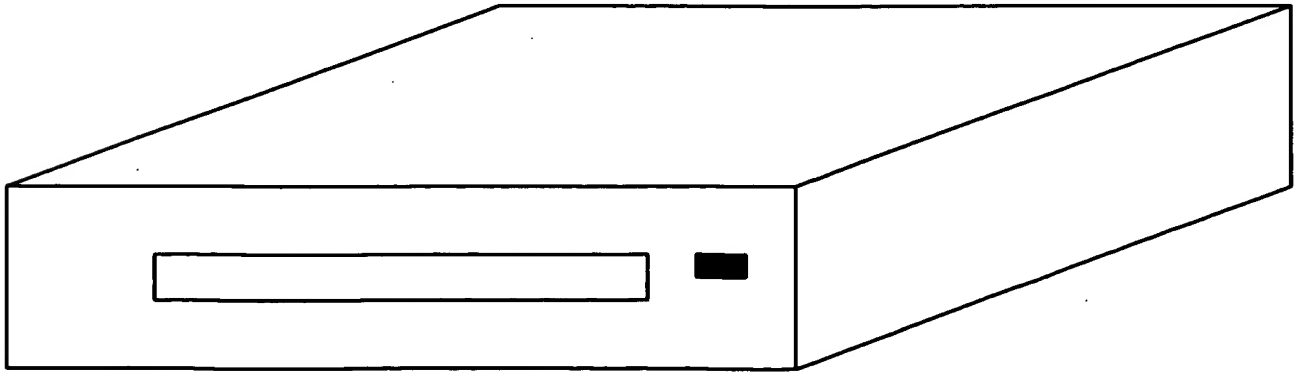


FIG. 55C
CD-RW Device

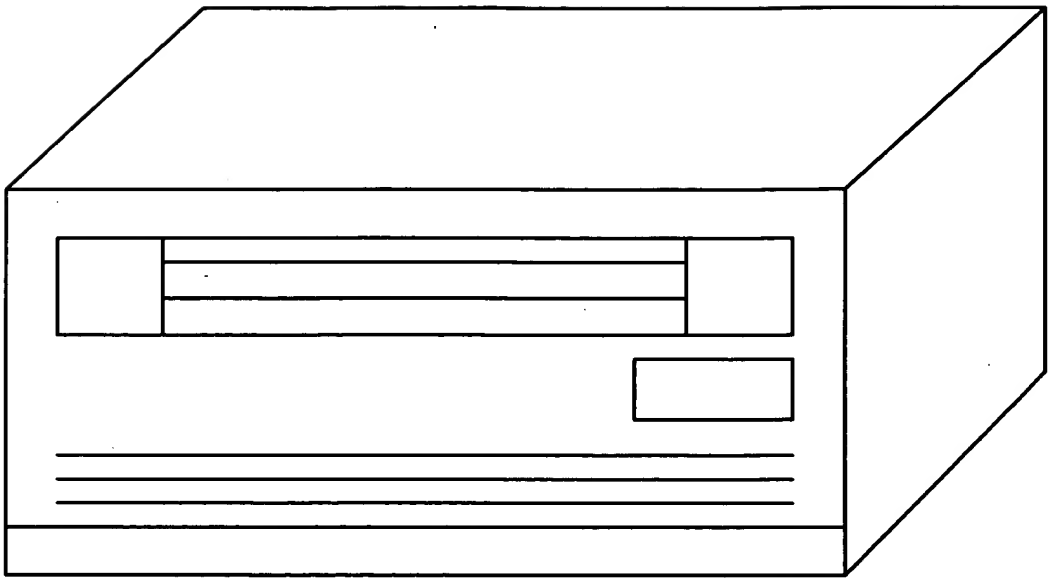


FIG. 56
Optical Data Recording Device

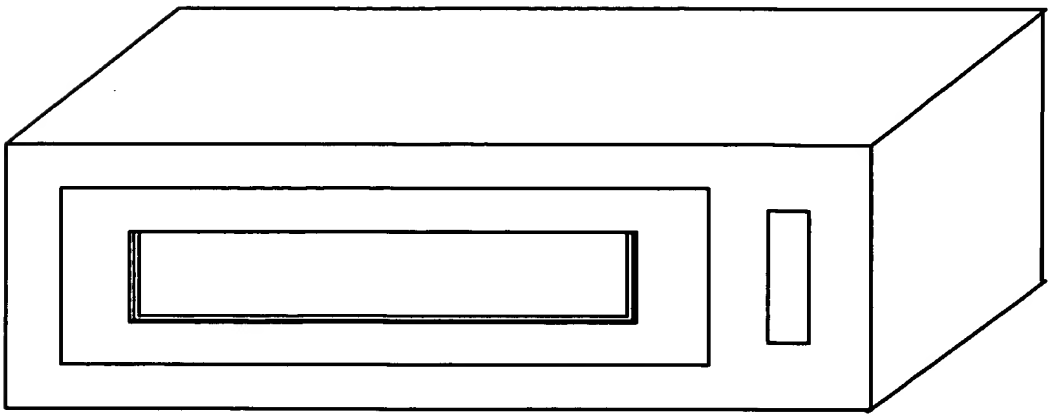


FIG. 57
Digital Audio Recording Device

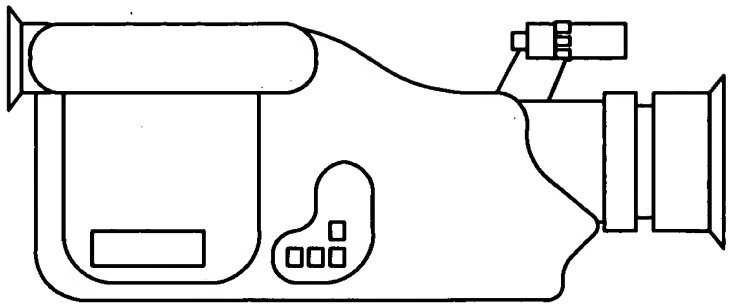


FIG. 58
Digital Camera

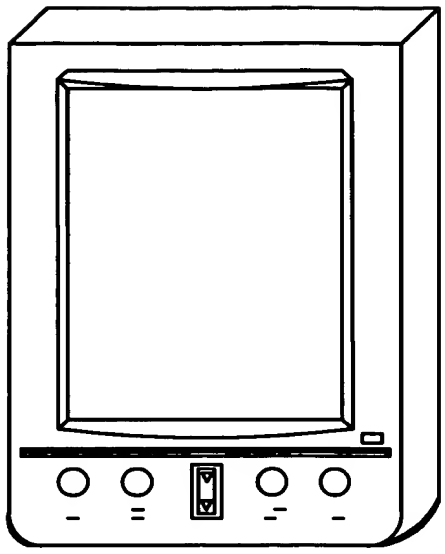


FIG. 59
PDA

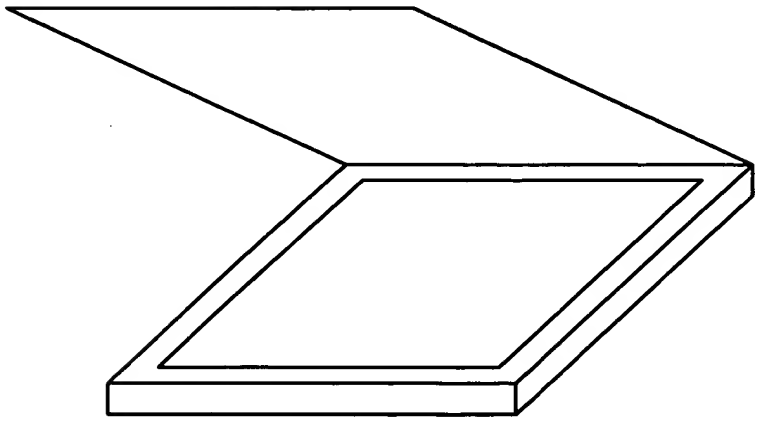


FIG. 60
Scanner

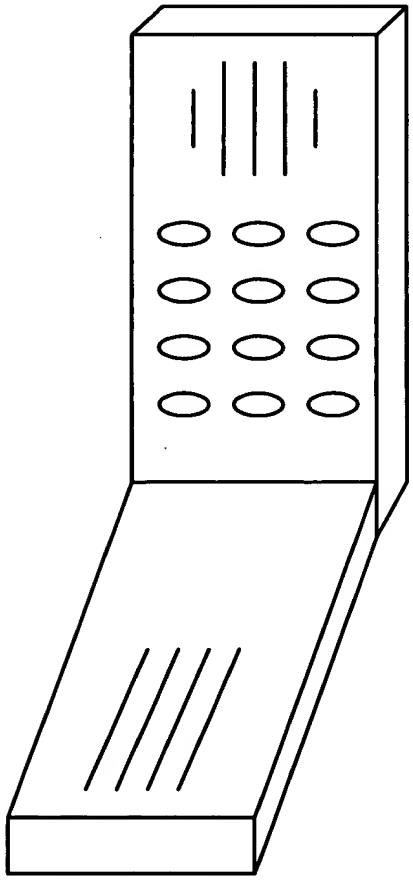


FIG. 61
Cellular Telephone

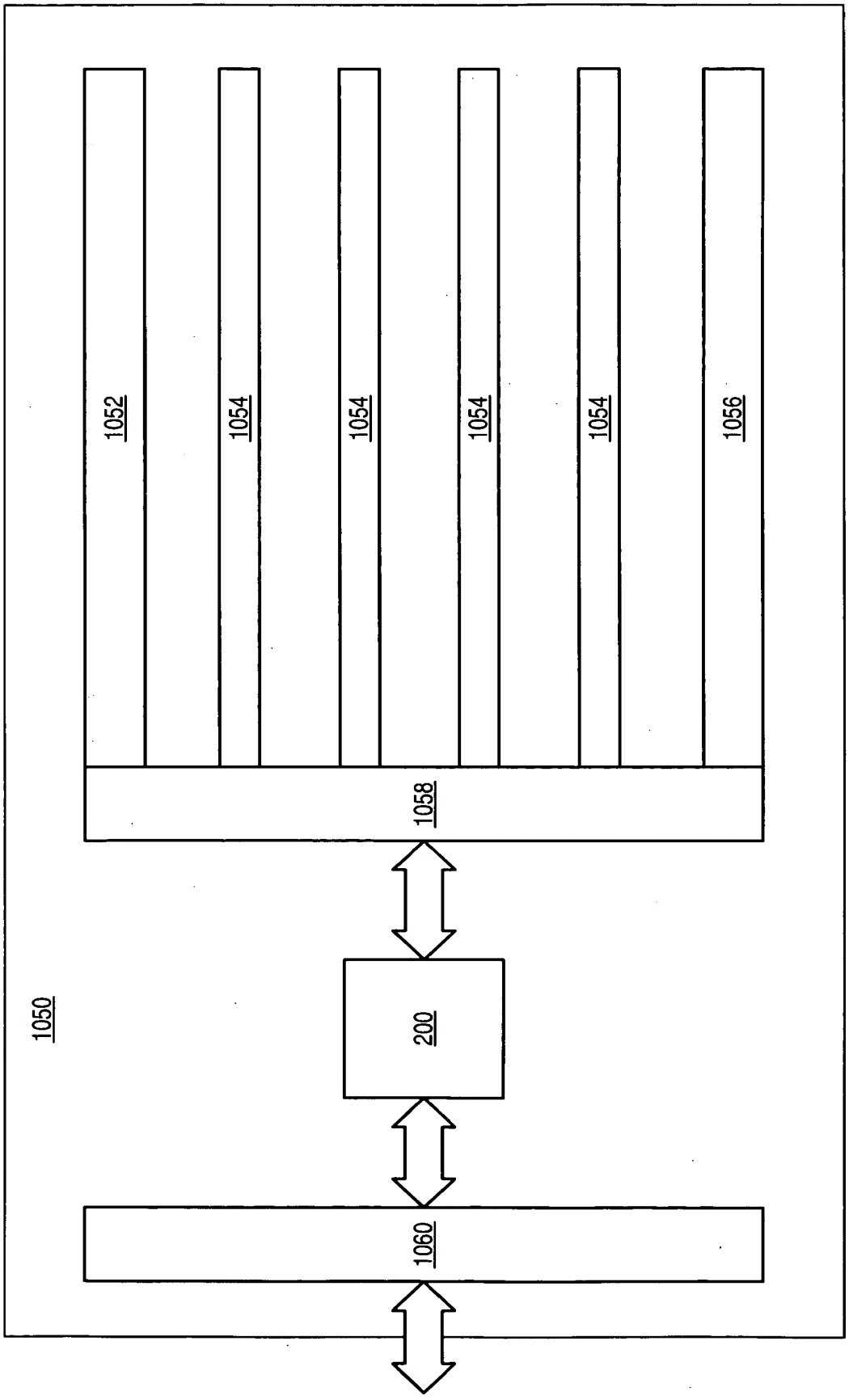


FIG. 62
Solid Sate Storage Device